ICL8018A/8019A/8020A
Quad Current Switch for D/A Conversion

FEATURES
- **TTL Compatible: LOW—0.8V HIGH—2.0V**
- **12 Bit Accuracy**
- **40 nsec, Switching Speed**
- **Wide Power Supply Range**
- **Low Temperature Coefficient**

APPLICATIONS:
- D/A-A/D Converters
- Digital Threshold Control
- Programmable Voltage Source
- Meter Drive
- X-Y Plotters

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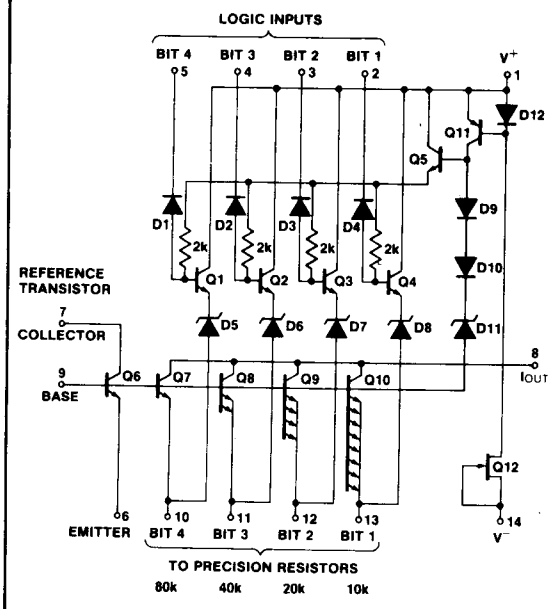
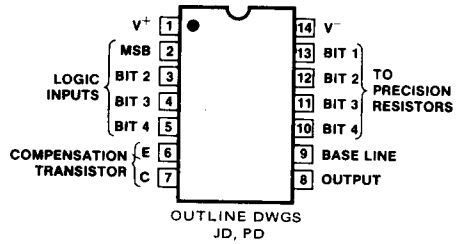
GENERAL DESCRIPTION
The Intersil ICL8018A family are high speed precision current switches for use in current summing digital-to-analog converters. They consist of four logically controlled current switches and a reference device on a single monolithic silicon chip. The reference transistor, combined with precision resistors and an external source, determines the magnitude of the currents to be summed. By weighting the currents in proportion to the binary bit which controls them, the total output current will be proportional to the binary number represented by the input logic levels.

The performance and economy of this family make them ideal for use in digital-to-analog converters for industrial process control and instrumentation systems.

SCHEMATIC DIAGRAM
EQUIVALENT CIRCUIT



PIN DIAGRAM



OUTLINE DWGS
JD, PD

ORDERING INFORMATION

ACCURACY	MILITARY TEMP RANGE CERDIP	COMMERCIAL TEMP RANGE PLASTIC DIP
Individual Devices		
.01%	ICL8018AMJD	ICL8018ACPD
0.1%	ICL8019AMJD	ICL8019ACPD
1.0%	ICL8020AMJD	ICL8020ACPD
Matched Sets*		
.01%	ICL8018AMXJD	ICL8018ACXPD
0.1%	ICL8019AMXJD	ICL8019ACXPD
1.0%	ICL8020AMXJD	ICL8020ACXPD

***NOTE:** Units ordered in equal quantities will be matched such that the V_{be}'s of the 8019 will be within ±10mV of the 8018 compensating transistor, and the V_{be}'s of the 8020 will be within ±50mV. The ICL8018 - X matched sets consist of one 8018, one 8019, and one 8020. The 8019 - X contains one 8019 and one 8020, while the 8020 - X contains two 8020's. Units shipped as matched sets will be marked with a unique set number.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Logic Input Voltage ..... −2V to V^+
Output Voltage ..... $V_{BASELINE}$ to +20V
$V_{BASELINE}$ ..... V^- to +5V
Storage Temperature ..... −65°C to +150°C
Operating Temperature ICL8018AM, ICL8019AM, ICL8020AM ..... −55°C to +125°C
ICL8018AC, ICL8019AC, ICL8010AC ..... 0°C to +70°C
Lead Temperature (soldering 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($4.5V \le V^+ \le 20V$, $V^- = -15V$, $T_A = 25°C$, V @ pin 6 = −5V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Error					
ICL8018A	V_{INHI} = 5.0V			±.01	
ICL8019A	V_{INLO} = 0.0V			±0.1	%
ICL8020A				±1	
Error Temperature Coefficient					
ICL8018A			± 2	± 5	ppm/°C
ICL8019A			± 2	± 25	
ICL8020A			± 2	± 50	
Settling Time To ± 1/2 LSB, R_L = 1kΩ					
8 BIT			100		
12 BIT			200		ns
Switching Time To Turn On LSB			40		ns
Output Current (Nominal)					
BIT 1 (MSB)			1.0		mA
BIT 2			0.5		
BIT 3			0.25		
BIT 4 (LSB)			0.125		
Zero Output Current	V_{IN} = 5.0V		10	50	nA
Output Voltage Range		$V_{BASELINE}$ +1V		+10	V
Input Coding-Complimentary Binary (See Truth Table)					
Logic Input Voltage	ΔI_{OUT} <400nA				
"0" (Switch ON)				0.8	V
"1" (Switch OFF)		2.0			
Logic Input Current					
"0"	V_{IN} = 0V		−1.0	−2	mA
"1" (into device)	V_{IN} = 5V		0.01	0.1	μA
Power Supply Rejection					
V^+			.005		%/V
V^-			.0005		
Supply Voltage Range					
V^+		4.5	5	20	V
V^-		−10	−15	−20	
Supply Current (V_{SUPP} = ±20V)					
I^+			7	10	mA
I^-			1	3	

BASIC D/A THEORY

The majority of digital to analog converters contain the elements shown in Figure 1. The heart of the D/A converter is the logic controlled switching network, whose output is an analog current or voltage proportional to the digital number on the logic inputs. The magnitude of the analog output is determined by the reference supply and the array of precision resistors, see fig. 2. If the switching network has a current output, often a transconductance amplifier is used to provide a voltage output.

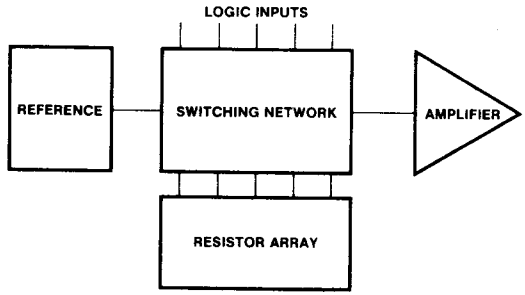


Figure 1: Elements of a D/A Converter

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Logic Input	Nominal Output Current (mA)
0 0 0 0	1.875
0 0 0 1	1.750
0 0 1 0	1.625
0 0 1 1	1.500
0 1 0 0	1.375
0 1 0 1	1.250
0 1 1 0	1.125
0 1 1 1	1.000
1 0 0 0	0.825
1 0 0 1	0.750
1 0 1 0	0.625
1 0 1*1	0.500
1 1 0 0	0.375
1 1 0 1	0.250
1 1 1 0	0.125
1 1 1 1	0.000

Figure 2: Truth Table

DEFINITION OF TERMS

The **resolution** of a D/A converter refers to the number of logic inputs used to control the analog output. For example, a D/A converter using two quad current sources would be an 8 bit converter. If three quads were used, a 12 bit converter would be formed. Resolution is often stated in terms of one part in, e.g., 256 since the number of controlling bits is related to total number of identifiable levels by the power of 2. The four bit quad has sixteen different levels (see Truth Table) each output corresponding to a particular logic input word.

Note that **maximum output** of the quad switch is $1 + 1/2 + 1/4 + 1/8 = 1\text{-}7/8 = 1.875$ mA. If this series of bits were continued as $1/16 + 1/32 + 1/64 \ldots\ldots$ $1/2^{(n-1)}$, the maximum output limit would approach 2.0 mA. This limiting value is called **full scale output**. The maximum output is always less than the full scale output by one least significant bit, LSB. For a twelve bit system (resolution 1 part in 4096) with a full scale output of 10.0 volts the maximum output would be $\frac{4095}{4096} \times 10V$. Since the numbers are extremely close for high resolution systems, the terms are often used interchangeably.

The **accuracy** of a D/A converter is generally taken to mean the largest error of any output level from its nominal value. The accuracy or **absolute error** is often expressed as a **percentage of the full scale output**.

Linearity relates the maximum error in terms of the deviation from the best straight line drawn through all the possible output levels. Linearity is related to accuracy by the scale factor and output offset. If the scale factor is exactly the nominal value and offset is adjusted to zero, then accuracy and linearity are identical. Linearity is usually specified as being within ±1/2 LSB of the best straight line.

Another desirable property of D/A converter is that it be **monotonic**. This simply implies that each successive output level is greater than the preceding one. A possible worst case condition would be when the output changes from most significant bit (MSB) OFF, all other bits ON to the next level which has the MSB ON and all other bits OFF, e.g., 10000 . . . to 01111.

In applications where a quad current switch drives a transconductance amplifier (current to voltage converter), transient response is almost exclusively determined by the output amplifier itself. Where the quad output current drives a resistor to ground, switching time and settling time are useful parameters.

Switching time is the familiar 10% to 90% rise time type of measurement. Low capacitance scope probes must be used to avoid masking the high speeds that current source switching affords. The **settling time** is the elapsed time between the application of a fast input pulse and the time at which the output voltage has settled to or approached its final value within a specified limit of accuracy. This limit of accuracy should be commensurate with the resolution of the DAC to be used.

Typically, the settling time specification describes how soon after an input pulse the output can be relied upon as accurate to within ±1/2 LSB of an N bit converter. Since the 8018A family has been desiged with all the collectors of the current switching transistors tied together, the output capacitance is constant. The transient response is, therefore, a simple exponential relationship, and from this the settling time can be calculated and related to the measured rise time as shown in Figure 3.

Bits of Resolution	±1/2 LSB Error % Full Scale	Number of Time Constants	Number of Rise Times
8	.2 %	6.2	2.8
10	.05%	7.6	3.4
12	.01%	9.2	4.2
Rise Time (10%-90%) = 2.2 R_L C_{eff}			

Figure 3: Settling Time vs. Rise Time Resistor Load

CIRCUIT OPERATION

An example of a practical circuit for the ICL8018A quad current switch is shown in Figure 4. The circuit can be analyzed in two sections; the first generates very accurate currents and the second causes these currents to be switched according to input logic signals. A reference current of 125μA is generated by a stable reference supply and a precision resistor. An op-amp with low offset voltage

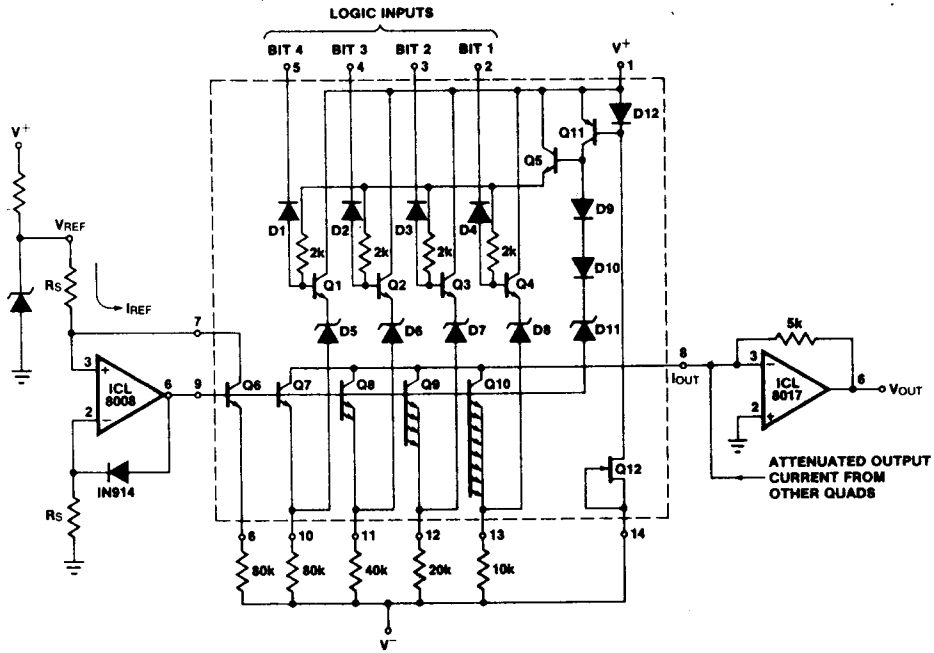


Figure 4: Typical Circuit

and low input bias current, such as the ICL8008, is used in conjunction with the internal reference transistor, Q_6, to force the voltage on the common base line, so that the collector current of Q_6 is equal to the reference current. The emitter current of Q_6 will be the sum of the reference current and a small base current causing a drop of slightly greater than 10 volts across the 80k resistor in the emitter of Q_6. Since this resistor is connected to −15V, this puts the emitter of Q_6 at nearly −5V and the common base line at one V_{BE} more positive at −4.35V typically.

Also connected to the common base line are the switched current source transistors Q_7 through Q_{10}. The emitters of these transistors are also connected through weighted precision resistors to −15V and their collector currents summed at pin 8. Since all these transistors, Q_6 through Q_{10}, are designed to have equal emitter-base voltages, it follows that all the emitter resistors will have equal voltage drops across them. It is this constant voltage and the precision resistors at the emitter that determine the exact value of switched output current. The emitter resistor of Q_7 is equal to that of Q_6, therefore, Q_7's collector current will be I_{REF} or 125μA. Q_8 has 40k in the emitter so that its collector current will be twice I_{REF} or 250μA. In the same way, the 20k and 10k in the emitters of Q_9 and Q_{10} contribute .5 mA and 1 mA to the total collector current.

The reference transistor and four current switching transistors are designed for equal emitter current density by making the number of emitters proportional to the current switched.

The remaining circuitry provides switching signals from the logic inputs. In the switch ON mode, zener diodes D_5 through D_8, connected to the emitter of each current switch transistor Q_7 thru Q_{10}, are reverse biased allowing the transistors to operate, producing precision currents summed in the collectors. The transistors are turned off by raising the voltage on the zeners high enough to turn on the zeners and raise the emitters of the switching transistor. This reverse biases the emitter base diode thereby shutting off that transistor's collector current.

The analog output current can be used to drive one load directly, (1kΩ to ground for FS = 1.875V for example) or can be used to drive a transconductance amplifier to give larger output voltages.

EXPANDING THE QUAD SWITCH

While there are few requirements for only 4 bit D to A converters, the 8018A is readily expanded to 8 and 12 bits with the addition of other quads and resistor dividers as shown in Figure 5.

To maintain the progression of binary weighted bit currents, the current output of the first quad drives the input of the transconductance amplifier directly, while a resistor divider network divides the output current of the second quad by 16 and the output current of the third by 256.

e.g., $I_{Total} = 1 \times (1 + 1/2 + 1/4 + 1/8) + 1/16(1 + 1/2 + 1/4 + 1/8) + 1/256(1 + 1/2 + 1/4 + 1/8) = 1 + 1/2 + 1/4 + 1/8 + 1/16 + 1/32 + 1/64 + 1/128 + 1/256 + 1/512 + 1/1024 + 1/2048.$

Note that each current switch is operating at the same high speed current levels so that standard 10k, 20k, 40k and 80k resistor networks can be used. Another advantage of this technique is that since the current outputs of the second and third quad are attenuated, so are the errors they contribute. This allows the use of less accurate switches and resistor networks in these positions; hence, the three accuracy grades of .01%, 0.1%, and 1% for the 8018A, 8019A and 8020A, respectively. It should be noted that only the reference transistor on the most significant quad is required to set up the voltage on the common base line joining the three sets of switching transistors (Pin 9).

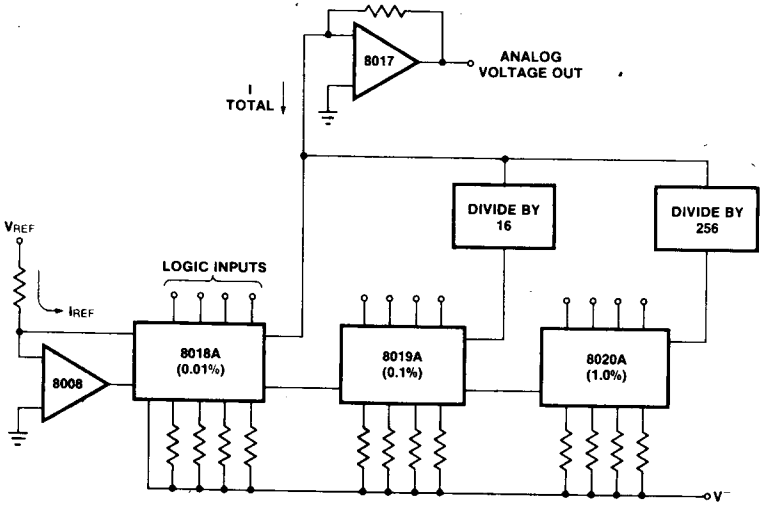


Figure 5: Expanding the Quad Switch

4 GENERATING REFERENCE CURRENTS — ZENER REFERENCE

As mentioned above, the 8018A switches currents determined by a constant voltage across the external precision resistors in the emitter of each switch. There are several ways of generating this constant voltage. One of the simplest is shown in Figure 6. Here an external zener diode is driven by the same current source line used to bias internal Zener D_{11}.

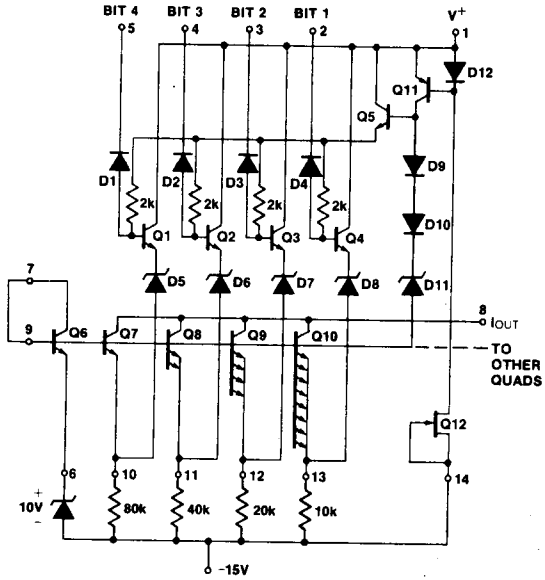


Figure 6: Simple Zener Reference

The zener current will be typically 1 mA per quad. The compensation transistor Q_6 is connected as a diode in series with the external zener. The V_{BE} of this transistor will approximately match the V_{BE}'s of the current switching transistors, thereby forcing the external zener voltage across each of the external resistors. The temperature coefficient of the external zener will dominate the temperature dependence of this scheme, however using a temperature compensated zener minimizes this problem. Since Q_6 is operating at a higher current density than the other switching transistors, the temperature matching of V_{BE}'s is not optimum, but should be adequate for a simple 8 or 10 bit converter.

The 8018A series is tested for accuracy with 10V reference voltage across the precision resistors, implying use of a 10 volt zener. Using a different external zener voltage will only slightly degrade accuracy if the zener voltage is above 5 or 6 volts.

When using other than 10 volt reference, the effects on logic thresholds should also be noted (see logic levels below). Full scale adjustment can be made at the output amplifier.

PNP REFERENCE

Another simple reference scheme is shown in Figure 7. Here an external PNP transistor is used to buffer a resistor divider. In this case, the −15 volt supply is used as a reference. Holding the V^- supply constant is not too difficult since the 8018A is essentially a constant current load. In this scheme, the internal compensation transistor is not necessary, since the V_{BE} matching is provided by the emitter-base junction of the external transistor. A small pot in series with the divider facilitates full scale output adjustment. A capacitor from base to collector of the external PNP will lower output impedance and minimize transient effects.

FULL COMPENSATION REFERENCE

For high accuracy, low drift applications, the reference scheme of Figure 4, offers excellent performance. In this circuit, a high gain op-amp compares two currents. The first is a reference current generated in R_S by the temperature compensated zener and the virtual ground at the non-inverting op-amp input. The second is the collector current of the reference transistor Q_6, provided on the quad switch. The output of the op-amp drives the base of Q_6 keeping its collector current exactly equal to the reference current. Since the switching transistor's emitter current densities are equal and since the precision resistors are proportional, all of the switched collector currents will have the proper value.

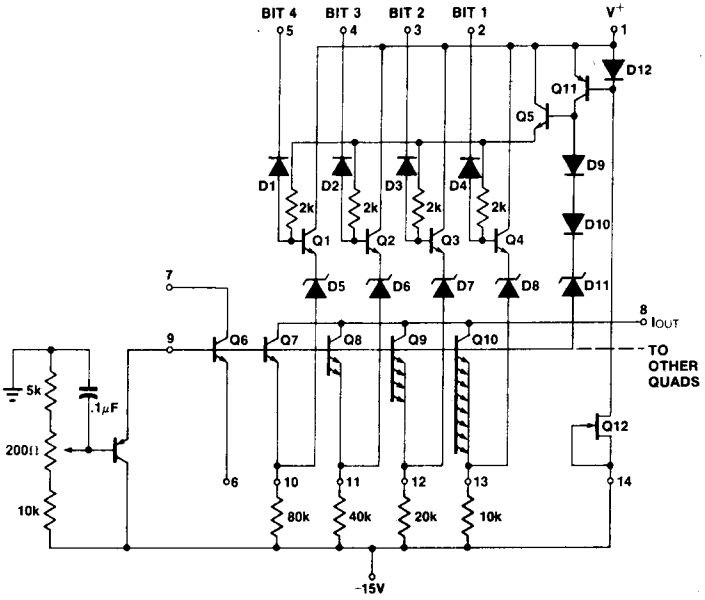
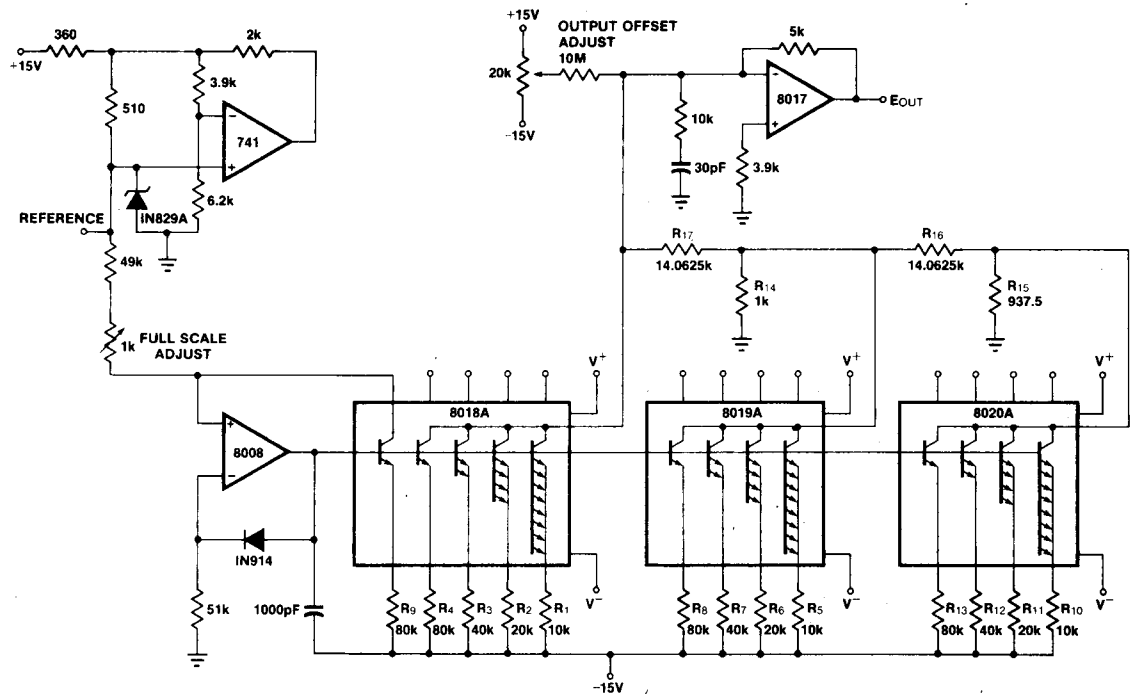


Figure 7: PNP Reference



NOTE: ALL RESISTORS RATIO TO R_1 UNLESS OTHERWISE NOTED.

TOLERANCE TABLE								
R_1	10k	0.1% ABS	R_6	20k	0.195%	R_{12}	40k	RATIO TO R_{10} 1%
R_2	20k	0.0122%	R_7	40k	0.391%	R_{13}	80k	RATIO TO R_{10} 1%
R_3	40k	0.0244%	R_8	80k	0.781%	R_{14}	1k	1% ABS
R_4	80k	0.0488%	R_9	80k	0.1%	R_{15}	937.5Ω	1% ABS
R_5	10k	0.096%	R_{10}	10k	0.5% ABS	R_{16}	14.0625k	RATIO TO R_{15} 1%
			R_{11}	20k	RATIO TO R_{10} 1%	R_{17}	14.0625k	RATIO TO R_{14} 0.1%

Figure 8

The op-amp feedback loop using the internal reference transistor will maintain proper currents in spite of V_{BE} drift, beta drift, resistor drift and changes in V^-. Using this circuit, temperature drifts of 2 ppm/°C are typical. A discrete diode connected as shown will keep Q_6 from saturating and prevent latch up if V^- is disconnected.

In any reference scheme, it is advisable to capacitively decouple the common base line to minimize transient effects. A capacitor, .001μF to .1μF from Pin 9 to analog ground is usually sufficient.

IMPROVED ACCURACY

As a final note on the subject of setting up reference levels, it should be pointed out that the largest contributor of error is the mismatch of V_{BE}'s of the current switching transistors. That is, if all the V_{BE}'s were identical, then all precision resistors would have exactly the same reference voltage across them. A one millivolt mismatch compared with ten volt reference across the precision resistors will cause a .01% error. While decreasing the reference voltage will decrease the accuracy, the voltage can be increased to achieve better than .01% accuracies. The voltage across the emitter resistors can be doubled or tripled with a proportional increase in resistor values resulting in improved absolute accuracy as well as improved temperature drift performance. This technique has been used successfully to implement up to 16 bit D/A converters.

4

PRACTICAL D/A CONVERTERS

The complete circuit for a high performance 12 bit D/A converter is shown in Figure 8. This circuit uses the "full compensation reference" described above to set the base line drive at the proper level, the temperature compensated zener is stabilized using an op-amp as a regulated supply, and the circuit provides a very stable, precise voltage reference for the D/A converter. The 16:1 and 256:1 resistor divider values are shown for a straight binary system; for a binary coded decimal system the dividers would be 10:1 and 100:1 (BCD is frequently encountered in building programmable voltage sources).

The analog output current of the 8018A current switches is converted to an output voltage using the 8017 as shown. The output amplifier must have low input bias current (small compared with the LSB current), low offset voltage and offset voltage drift, high slew rate and fast settling time. The input compensation shown helps improve pulse response by providing a finite impedance at high frequencies for a point that is virtual ground at DC.

An alternative bias scheme is shown in Figure 9. In this case, the bias at the common base line is fixed by inverting op-amp A_4, the gain of which is adjusted to give −5.0 volts at the emitter of the reference transistor. With the bias at the common base line fixed, the regular circuit of A_1 uses the internal reference transistor and drives the bus connecting all the precision resistors. This isolates the precision resistors from V^- fluctuations. Zener D_3 and constant current source Q_1 keep the regulating 8008 op-amp in mid-range. There are several alternative bias schemes depending on power supplies available. If −20 volts is used for V^-, the bottom of the precision resistor will be at −15 and operation will be the same as the standard circuit. If only −15V is available for V^- the gain of the output transconductance amplifier can be increased by 30% to allow use of a smaller switching currents with 7 volts across the precision resistors.

MULTIPLYING DAC

The circuit of Figure 9 is also convenient to use as a one quadrant multiplying D/A converter. In a multiplying DAC, the analog output is proportional to the product of a digital number and an analog signal. The digital number drives the logic inputs, while the analog signal replaces the constant reference voltage, and produces a current to set up the regulating 8008 op-amp. To vary the magnitude of currents being switched, the voltage across all the 10k, 20k, 40k and 80k resistors must be modulated according to the analog input. An analog input of 0 to +10 volts and an 80k resistor at the input to the 8008 will fulfill this requirement.

CALIBRATING THE 12 BIT D/A CONVERTER

1. With all logic inputs high (ones) adjust the output amplifier offset for zero volts out.
2. Put in the word 0000 1111 1111 (Quad 1 maximum output Quad 2 and 3 off) and adjust full scale pot for V_O of 15/16 (10V) where full scale output is to be 10 volts.
3. Put in the word 1111 0000 1111 and trim the Quad 2 divider for V_O of 15/256 (10V). This adjustment compensates for V_{BE} mismatches between quads although matched sets are available (see data sheet).
4. Put in the word 1111 1111 0000 and trim the Quad 3 divider for V_O of 15/4096 (10V).
5. Finally, with all bits ON (all 0's) readjust the full scale factor pot for

$$V_O = 4095/4096\ (10V)$$

SYSTEM INTERFACE REQUIREMENTS

Using the 8018A series in practical circuits requires consideration of the following interface requirements.

Logic Levels: The 8018A is designed to be compatible with TTL, DTL and RTL logic drive systems. The one constraint imposed on the external voltage levels is that the emitters of the conducting current switch transistors be in the vicinity of −5V; this will be the same as the voltage on Pin 6 if the reference transistor is used. When using other than −5V at Pin 6, the direct bearing on logic threshold should be considered.

Power Supplies: One advantage of the ICL8018A is its tolerance of a wide range of supply voltage. The positive supply voltage need only be large enough (greater than +4.5V) to keep Q_{11} out of saturation, and the negative supply needs to be more negative than −10V to ensure constant current operation of Q_{12}. The maximum supply voltage of ±20V is dictated by transistor breakdown voltages. It is often convenient to use ±15V supplies in systems with op-amps and other I.C.'s. These supplies tend to be better regulated and free from high current transients found on supplies used to power TTL Logic. As with any high speed circuit, attention to layout and adequate power supply decoupling will minimize switching effects.

Ground: High resolution D/A, e.g., 12 bits require fairly large logic drive currents. The change from all bits ON to all bits OFF is a considerable change in supply current being returned to ground. Because of this, it is usually advisable to maintain separate ground points for the analog and digital sections.

Resistors: Each quad current switch requires a set of matched resistors scaled proportional to their binary currents as R, 2R, 4R and 8R. For a 10V resistor voltage drop and "2 mA" full scale output current, resistor values of 10k, 20k, 40k and 80k are convenient. Other resistor values can be used, for example, to increase total output current. The

individual switched currents can be increased up to 100% of their nominal values. The overall accuracy of the complete D/A converter depends on the accuracy of the reference, the accuracy of the quad current switch and tolerance of resistor matching. Because of the binary progression of switched currents, the tolerance of 80k/10k match can be twice that of the 40k/10k which, in turn, can be twice the tolerance of the 20k/10k ratio and still have equal output current errors. The current dividers between quads allows use of less well matched sets of resistors further along in the D/A just as it allows use of .01%, 0.1%, and 1% accurate quad current switches. There are several manufacturers producing the complete precision resistor networks required to implement up to 12 bit D/A converters. Contact Intersil for additional information.*

*Resistor Ladder Networks are manufactured by the following companies:

Micro Networks Corporation
5 Barbara Lane
Worcester, Massachusetts 01604
Tel. (617) 756-4635

Allen-Bradley Company
1201 S. Second Street
Milwaukee, Wisconsin 53204
Tel. (414) 671-2000

Hycomp, Inc.
146 Main Street
Maynard, Massachusetts 01754
Tel. (617) 897-4578

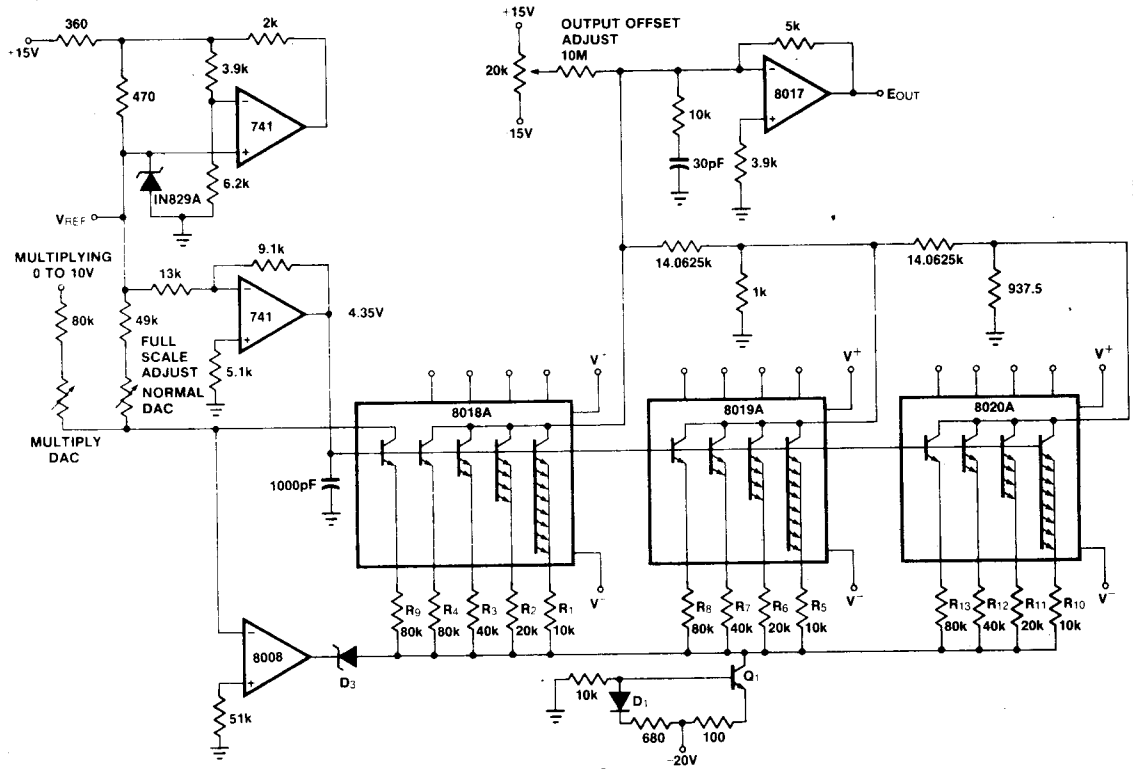


Figure 9

For further information see the following Applications Bulletins.

A016 "Selecting A/D Converters" by Dave Fullagar.
A018 "Do's and Don'ts of Applying A/D Converters" by Peter Bradshaw and Skip Osgood.
A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger.