National Semiconductor

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LMH7324

Quad 700 ps High Speed Comparator with RSPECL Outputs

General Description

The LMH7324 is a quad comparator with 700 ps propagation delay and low dispersion of 20 ps for a supply voltage of 5V. The input voltage range extends 200 mV below the negative supply. This enables the LMH7324 to ground sense even when operating on a single power supply. The device operates from a wide supply voltage range from 5V to 12V, which allows for a wide input voltage range. However, if a wide input voltage range is not required, operating from a single-ended 5V supply results in a significant power savings, and less heat dissipation.

The outputs of the LMH7324 are RSPECL compatible and can also be configured to create LVDS levels. The LMH7324 operates over the industrial temperature range of −40°C to 125°C. The LMH7324 is available in a 32-Pin LLP package.

Features

($V_{CCI} = V_{CCO} = +5V$, $V_{EE} = 0V$.)

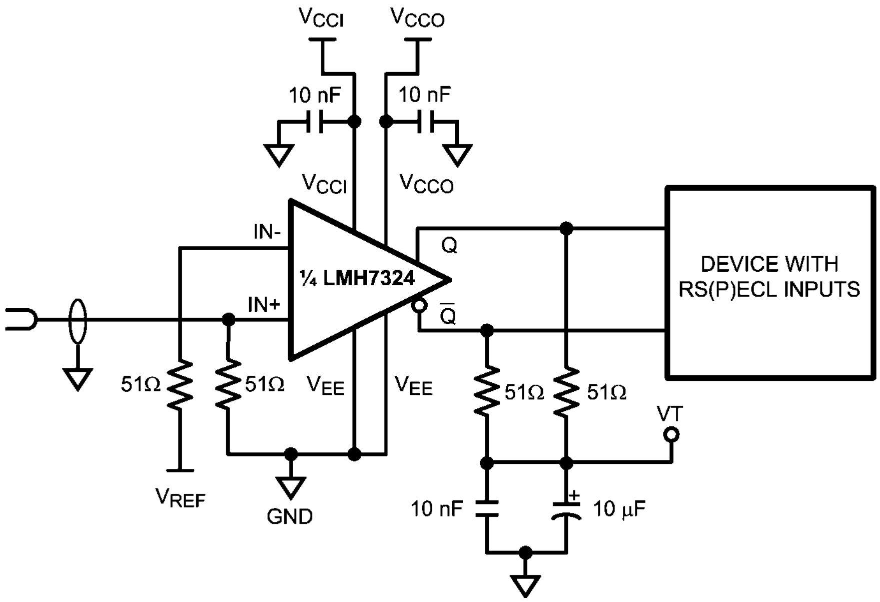
■ Propagation delay	700 ps
■ Overdrive dispersion	20 ps
■ Fast rise and fall times	150 ps
■ Supply range	5V to 12V

- Input common mode range extends 200 mV below negative rail
- RSPECL outputs

Applications

- Digital receivers
- High speed signal restoration
- Zero-crossing detectors
- High speed sampling
- Window comparators
- High speed signal triggering

Typical Application



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2.5 kV
Machine Model	250V
Output Short Circuit Duration	(Note 3, Note 4)
Supply Voltages ($V_{CCx} - V_{EE}$)	13.2V
Voltage at Input/Output Pins	±13V
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	+150°C

Operating Ratings (Note 1)

Supply Voltage ($V_{CCx} - V_{EE}$)	5V to 12V
Temperature Range	−40°C to +125°C
Package Thermal Resistance	
32-Pin LLP	36°C/W

12V DC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for $T_J = 25°C$. $V_{CCI} = V_{CCO} = 12V$, $V_{EE} = 0V$, $R_L = 50\Omega$ to V_{CCO}-2V, $V_{CM} = 300$ mV. (Note 7)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Input Characteristics						
I_B	Input Bias Current (Note 11)	V_{IN} Differential = 0V	−5	−2.5		μA
I_{OS}	Input Offset Current	V_{IN} Differential = 0V	−250	40	250	nA
TC I_{OS}	Input Offset Current TC (Note 10)	V_{IN} Differential = 0V		0.15		nA/°C
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−9.5		+9.5	mV
TC V_{OS}	Input Offset Voltage TC (Note 10)	V_{CM} = 0V		7		μV/°C
V_{RI}	Input Voltage Range	CMRR > 50 dB	V_{EE}		V_{CCI}−2	V
V_{RID}	Input Differential Voltage Range	$V_{EE} \le$ INP or INM $\le V_{CCI}$	−12		+12	V
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le V_{CC}-2V$		83		dB
PSRR	Power Supply Rejection Ratio	$V_{CM} = 0V$, $5V \le V_{CC} \le 12V$		75		dB
A_V	Active Gain			54		dB
Hyst	Hysteresis	Fixed Internal Value		20.8		mV
Output Characteristics						
V_{OH}	Output Voltage High	V_{IN} Differential = 25 mV	10.78	10.85	10.93	V
V_{OL}	Output Voltage Low	V_{IN} Differential = 25 mV	10.43	10.50	10.58	V
V_{OD}	Output Voltage Differential	V_{IN} Differential = 25 mV	300	345	400	mV
Power Supplies						
I_{VCCI}	V_{CCI} Supply Current/Channel	V_{IN} Differential = 25 mV		5.6	8	mA
I_{VCCO}	V_{CCO} Supply Current/Channel	V_{IN} Differential = 25 mV		11.6	17	

12V AC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for $T_J = 25°C$. $V_{CCI} = V_{CCO} = 12V$, $V_{EE} = 0V$, $R_L = 50\Omega$ to V_{CCO}-2V, $V_{CM} = 300$ mV. (Note 7)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
TR	Maximum Toggle Rate	Overdrive = ±50 mV, C_L = 2 pF @ 50% Output Swing		3.84		Gb/s
	Minimum Pulse Width	Overdrive = ±50 mV, C_L = 2 pF @ 50% Output Swing		280		ps
$t_{jitter\text{-}RMS}$	RMS Random Jitter	Overdrive = ±100 mV, C_L = 2 pF Center Frequency = 140 MHz Bandwidth = 10 Hz–20 MHz		615		fs

Symbol	Parameter	Conditions	Min (*Note 6*)	Typ (*Note 5*)	Max (*Note 6*)	Units
t_{PDH}	Propagation Delay (see *Figure 3* application note) Input SR = Constant V_{IN} Startvalue = V_{REF} −100 mV	Overdrive 20 mV		737		ps
		Overdrive 50 mV		720		
		Overdrive 100 mV		706		
		Overdrive 1V		731		
$t_{OD\text{-}disp}$	Input Overdrive Dispersion	t_{PDH} @ Overdrive 20 mV ↔ 100 mV		31		ps
		t_{PDH} @ Overdrive 100 mV ↔ 1V		25		
$t_{SR\text{-}disp}$	Input Slew Rate Dispersion	0.1 V/ns to 1 V/ns Overdrive 100 mV		40		ps
$t_{CM\text{-}disp}$	Input Common Mode Dispersion	SR = 1 V/ns, Overdrive 100 mV, $0V \leq V_{CM} \leq V_{CCI} - 2V$		28		ps
Δt_{PDLH}	Q to $\overline{Q}$ Time Skew $\mid t_{PDH} - t_{PD\overline{L}} \mid$ (*Note 8*)	Overdrive = 50 mV, C_L = 2 pF		55		ps
Δt_{PDHL}	Q to $\overline{Q}$ Time Skew $\mid t_{PDL} - t_{PD\overline{H}} \mid$ (*Note 8*)	Overdrive = 50 mV, C_L = 2 pF		40		ps
t_r	Output Rise Time (20% - 80%) (*Note 9*)	Overdrive = 50 mV, C_L = 2 pF		140		ps
t_f	Output Fall Time (20% - 80% (*Note 9*)	Overdrive = 50 mV, C_L = 2 pF		140		ps

5V DC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = 25°C. $V_{CCI} = V_{CCO}$ = 5V, V_{EE} = 0V, R_L = 50Ω to V_{CCO}-2V, V_{CM} = 300 mV. (*Note 7*)

Symbol	Parameter	Conditions	Min (*Note 6*)	Typ (*Note 5*)	Max (*Note 6*)	Units
I_B	Input Bias Current (*Note 11*)	V_{IN} Differential = 0V	−5	−2.2		µA
I_{OS}	Input Offset Current	V_{IN} Differential = 0V	−250	30	+250	nA
TC I_{OS}	Input Offset Current TC (*Note 10*)	V_{IN} Differential = 0V		0.1		nA/°C
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−9.5		+9.5	mV
TC V_{OS}	Input Offset Voltage TC (*Note 10*)	V_{CM} = 0V		7		µV/°C
V_{RI}	Input Voltage Range	CMRR > 50 dB	V_{EE}		V_{CCI}−2	V
V_{RID}	Input Differential Voltage Range	$V_{EE} \leq$ INP or INM $\leq V_{CCI}$	−5		+5	V
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq V_{CC}-2V$		80		dB
PSRR	Power Supply Rejection Ratio	V_{CM} = 0V, $5V \leq V_{CC} \leq 12V$		75		dB
A_V	Active Gain			54		dB
Hyst	Hysteresis	Fixed Internal Value		22.5		mV
Output Characteristics						
V_{OH}	Output Voltage High	V_{IN} Differential = 25 mV	3.8	3.87	3.95	V
V_{OL}	Output Voltage Low	V_{IN} Differential = 25 mV	3.45	3.52	3.60	V
V_{OD}	Output Voltage Differential	V_{IN} Differential = 25 mV	300	345	400	mV
Power Supplies						
I_{VCCI}	V_{CCI} Supply Current/Channel	V_{IN} Differential = 25 mV		5.4	7.5	mA
I_{VCCO}	V_{CCO} Supply Current/Channel	V_{IN} Differential = 25 mV		11	15	mA

5V AC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for $T_J = 25°C$. $V_{CCI} = V_{CCO} = 5V$, $V_{EE} = 0V$, $R_L = 50\Omega$ to V_{CCO}-2V, $V_{CM} = 300$ mV. (Note 7)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
TR	Maximum Toggle Rate	Overdrive = ±50 mV, $C_L = 2$ pF @ 50% Output Swing		3.72		Gb/s
	Minimum Pulse Width	Overdrive = ±50 mV, $C_L = 2$ pF @ 50% Output Swing		290		ps
$t_{jitter\text{-}RMS}$	RMS Random Jitter	Overdrive = ±100 mV, $C_L = 2$ pF Center Frequency = 140 MHz Bandwidth = 10 Hz–20 MHz		602		fs
t_{PDH}	Propagation Delay (see Figure 3 application note)	Overdrive 20 mV		740		ps
		Overdrive 50 mV		731		
	Input SR = Constant V_{IN} Startvalue = V_{REF} −100 mV	Overdrive 100 mV		722		
		Overdrive 1V		740		
$t_{OD\text{-}disp}$	Input Overdrive Dispersion	T_{PDH} @ Overdrive 20 mV ↔ 100 mV		18		ps
		T_{PDH} @ Overdrive 100 mV ↔ 1V		19		
$t_{SR\text{-}disp}$	Input Slew Rate Dispersion	0.1 V/ns to 1 V/ns, Overdrive = 100 mV		40		ps
$t_{CM\text{-}disp}$	Input Common Mode Dispersion	SR = 1 V/ns, Overdrive 100 mV, $0V \leq V_{CM} \leq V_{CCI} - 2V$		24		ps
$\Delta t_{PDLH\text{-}disp}$	Q to $\overline{Q}$ Time Skew $\mid t_{PDH} - t_{PD\overline{L}} \mid$ (Note 8)	Overdrive = 50 mV, $C_L = 2$ pF		60		ps
Δt_{PDHL}	Q to $\overline{Q}$ Time Skew $\mid t_{PDL} - t_{PD\overline{H}} \mid$ (Note 8)	Overdrive = 50 mV, $C_L = 2$ pF		40		ps
t_r	Output Rise Time (20% - 80%) (Note 9)	Overdrive = 50 mV, $C_L = 2$ pF		145		ps
t_f	Output Fall Time (20% - 80%) (Note 9)	Overdrive = 50 mV, $C_L = 2$ pF		145		ps

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate specifications for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)
Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC)

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 4: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$.

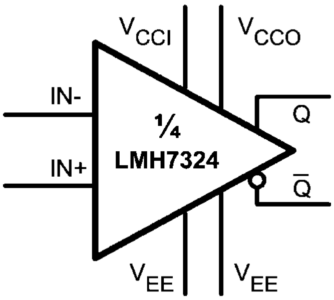
Note 8: Propagation Delay Skew, Δt_{PD}, is defined as the average of Δt_{PDLH} and Δt_{PDHL}.

Note 9: The rise or fall time is the average of the Q and $\overline{Q}$ rise or fall time.

Note 10: Average Temperature Coefficient is determined by dividing the change in a parameter at temperature extremes by the total temperature change.

Note 11: Positive current corresponds to current flowing into the device.

Connection Diagram



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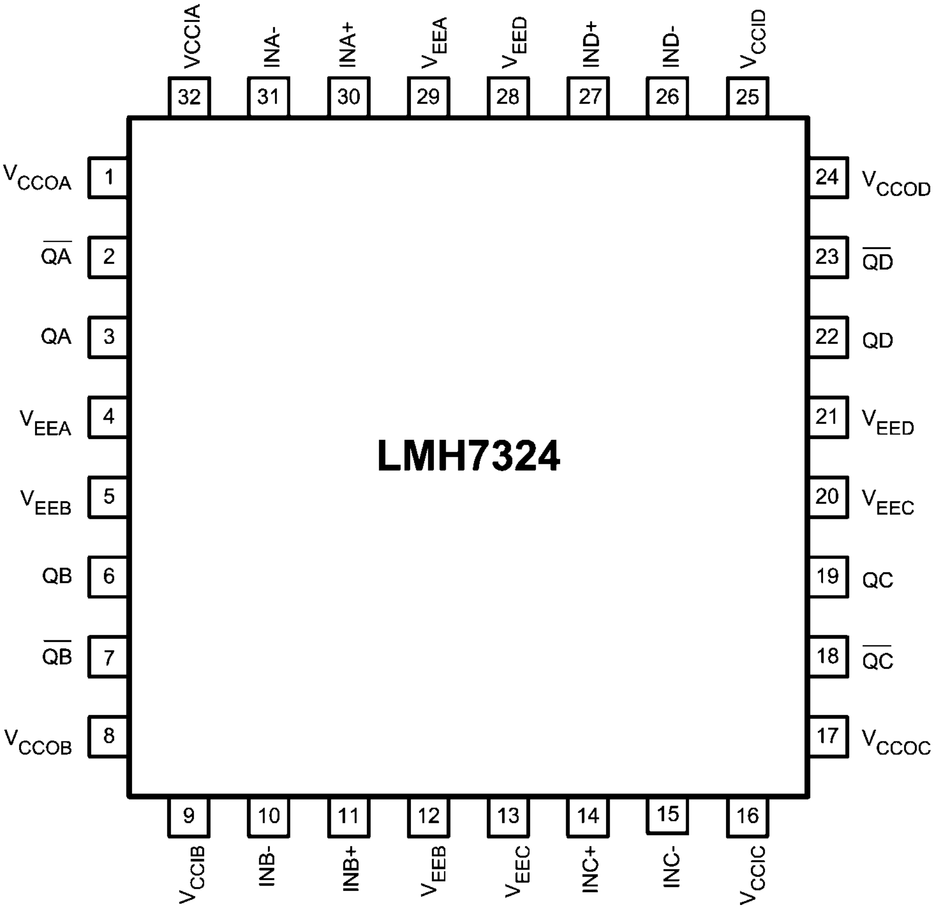
32-Pin LLP



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Top View

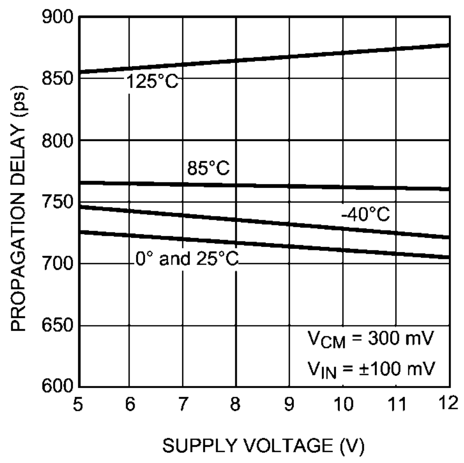
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
32-Pin LLP	LMH7324SQ	L7324SQ	1k Units Tape and Reel	SQA32A
	LMH7324SQX		4.5k Units Tape and Reel	

Typical Performance Characteristics

At T_J = 25°C, V^+ = +5V, V^- = 0V, unless otherwise specified.

Propagation Delay vs. Supply Voltage



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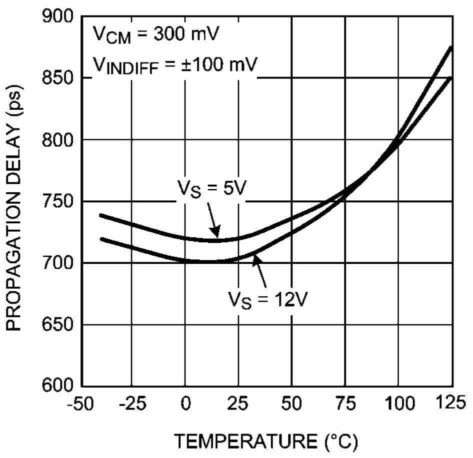
Propagation Delay vs. Temperature



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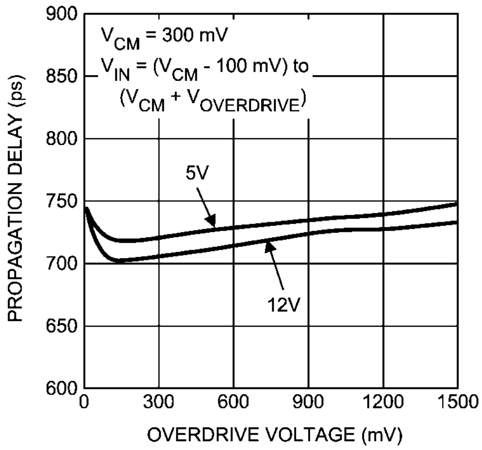
Propagation Delay vs. Overdrive Voltage



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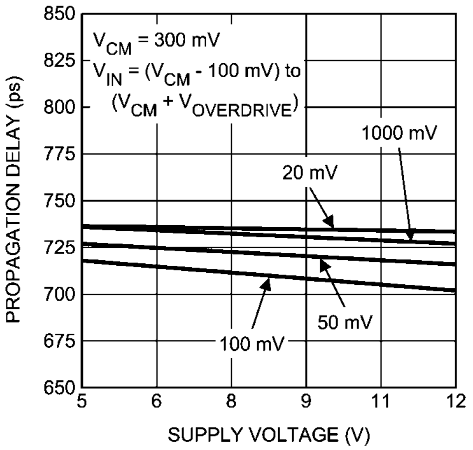
Propagation Delay vs. Supply Voltage for Different Overdrive



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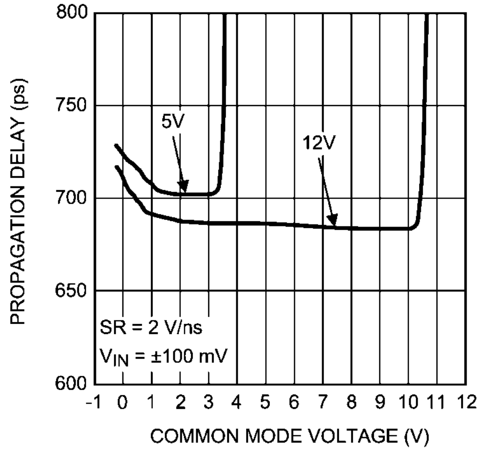
Propagation Delay vs. Common Mode Voltage



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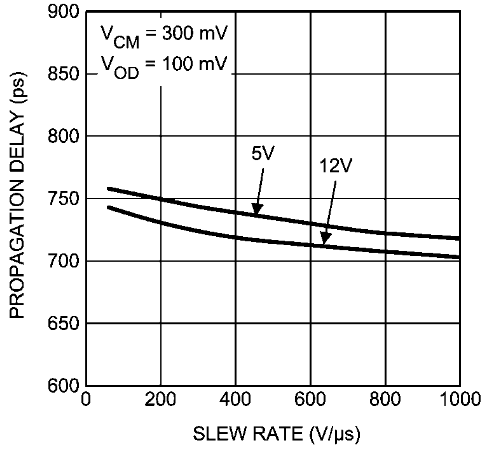
Propagation Delay vs. Slew Rate



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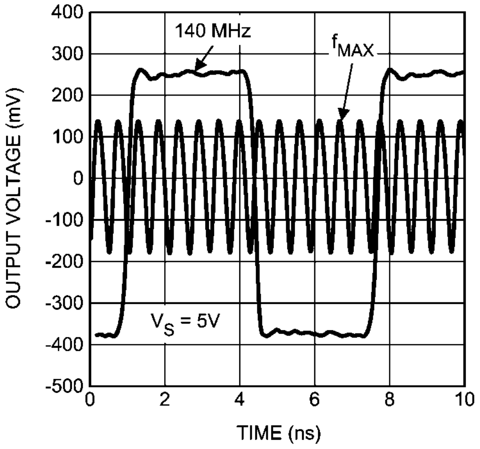
Pulse Response and Maximum Toggle Rate



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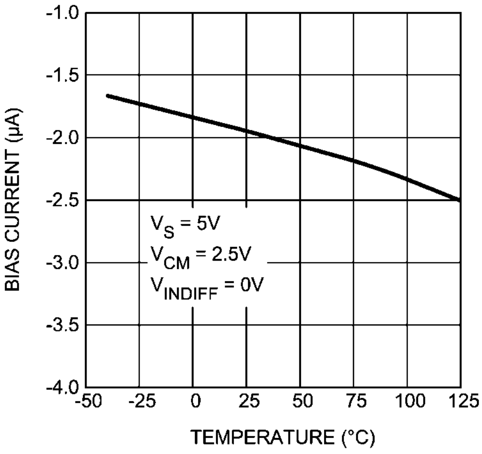
Bias Current vs. Temperature



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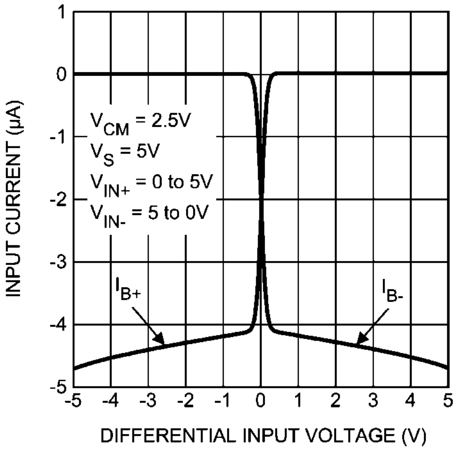
Input Current vs. Differential Input Voltage



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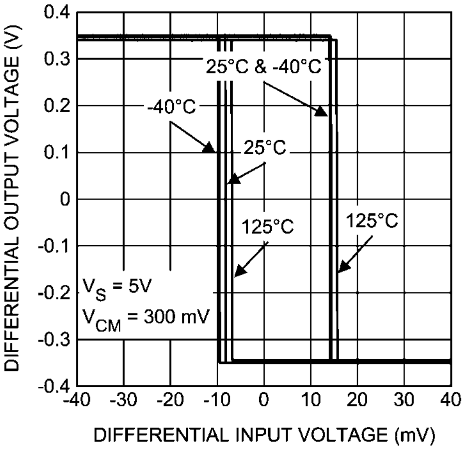
Output Voltage vs. Input Voltage



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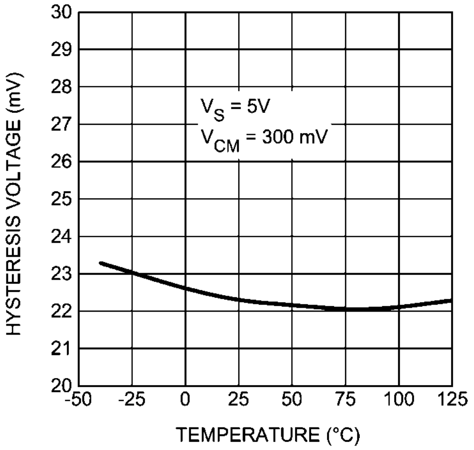
Hysteresis Voltage vs. Temperature



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Application Information

INTRODUCTION

The LMH7324 is a high speed comparator with RS(P)ECL (**R**educed **S**wing **P**ositive **E**mitter **C**oupled **L**ogic) outputs, and is compatible with LVDS (**L**ow **V**oltage **D**ifferential **S**ignaling) if V_{CCO} is set to 2.5V. The use of complementary outputs gives a high level of suppression for common mode noise. The very fast rise and fall times of the LMH7324 enable data transmission rates up to several Gigabits per second (Gbps). The LMH7324 inputs have a common mode voltage range that extends 200 mV below the negative supply voltage thus allowing ground sensing when used with a single supply. The rise and fall times of the LMH7324 are about 150 ps, while the propagation delay time is about 700 ps. The LMH7324 can operate over the supply voltage range of 5V to 12V, while using single or dual supply voltages. This is a flexible way to interface between several high speed logic families. Several configurations are described in the section INTERFACE BETWEEN LOGIC FAMILIES. The outputs are referenced to the positive V_{CCO} supply rail. The supply current is 17 mA at 5V (per comparator, load current excluded.) The LMH7324 is offered in a 32-Pin LLP package. This small package is ideal where space is an important issue.

INPUT & OUTPUT TOPOLOGY

All input and output pins are protected against excessive voltages by ESD diodes. These diodes are conducting from the negative supply to the positive supply. As can be seen in *Figure 1*, both inputs are connected to these diodes. Protection against excessive supply voltages is provided by two power clamps per comparator: one between the V_{CCI} and the V_{EE} and one between the V_{CCO} and the V_{EE}.

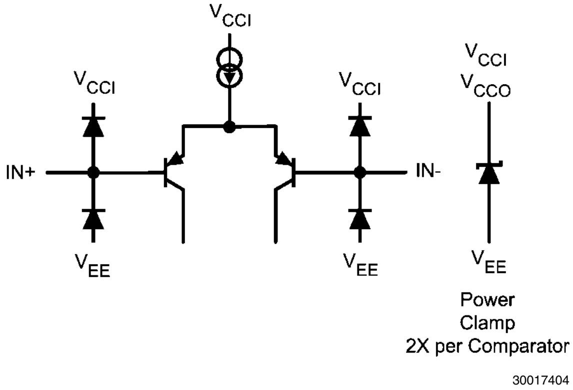

FIGURE 1. Equivalent Input Circuitry

The output stage of the LMH7324 is built using two emitter followers, which are referenced to the V_{CCO}. (See *Figure 2*.) Each of the output transistors is active when a current is flowing through any external output resistor connected to a lower supply rail. Activating the outputs is done by connecting the emitters to a termination voltage which lies 2V below the V_{CCO}. In this case a termination resistor of 50Ω can be used and a transmission line of 50Ω can be driven. Another method is to connect the emitters through a resistor to the most negative supply by calculating the right value for the emitter current in accordance with the datasheet tables. Both methods are useful, but they each have good and bad aspects.

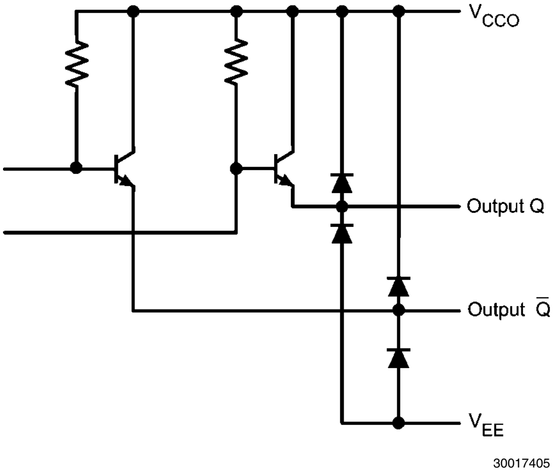

FIGURE 2. Equivalent Output Circuitry

The output voltages for ‘1’ and ‘0’ have a difference of approximately 400 mV and are respectively 1.1V (for the ‘1’) and 1.5V (for the ‘0’) below the V_{CCO}. This swing of 400 mV is enough to drive any LVDS input but can also be used to drive any ECL or PECL input, when the right supply voltage is chosen, especially the right level for the V_{CCO}.

DEFINITIONS

This table provides a short description of the parameters used in the datasheet and in the timing diagram of *Figure 3*.

Symbol	Text	Description
I_B	Input Bias Current	Current flowing in or out of the input pins, when both are biased at the V_{CM} voltage as specified in the tables.
I_{OS}	Input Offset Current	Difference between the input bias current of the inverting and non-inverting inputs.
TC I_{OS}	Average Input Offset Current Drift	Temperature coefficient of I_{OS}.
V_{OS}	Input Offset Voltage	Voltage difference needed between IN+ and IN– to make the outputs change state, averaged for H to L and L to H transitions.
TC V_{OS}	Average Input Offset Voltage Drift	Temperature coefficient of V_{OS}.
V_{RI}	Input Voltage Range	Voltage which can be applied to the input pin maintaining normal operation.
V_{RID}	Input Differential Voltage Range	Differential voltage between positive and negative input at which the input clamp is not working. The difference can be as high as the supply voltage but excessive input currents are flowing through the clamp diodes and protection resistors.
CMRR	Common Mode Rejection Ratio	Ratio of input offset voltage change and input common mode voltage change.
PSRR	Power Supply Rejection Ratio	Ratio of input offset voltage change and supply voltage change from V_{S-MIN} to V_{S-MAX}.
A_V	Active Gain	Overall gain of the circuit.
Hyst	Hysteresis	Difference between the switching point ‘0’ to ‘1’ and vice versa.
V_{OH}	Output Voltage High	High state single ended output voltage ($\overline{Q}$ or Q). (See *Figure 17*)
V_{OL}	Output Voltage Low	Low state single ended output voltage ($\overline{Q}$ or Q). (See *Figure 17*)
V_{OD}	Average of V_{ODH} and V_{ODL}	$(V_{ODH} + V_{ODL})/2$
I_{VCCI}	Supply Current Input Stage	Supply current into the input stage.
I_{VCCO}	Supply Current Output Stage	Supply current into the output stage while current through the load resistors is excluded.
I_{VEE}	Supply Current V_{EE} Pin	Current flowing out of the negative supply pin.
TR	Maximum Toggle Rate	Maximum frequency at which the outputs can toggle at 50% of the nominal V_{OH} and V_{OL}.
PW	Pulse Width	Time from 50% of the rising edge of a signal to 50% of the falling edge.
t_{PDH} resp t_{PDL}	Propagation Delay	Delay time between the moment the input signal crosses the switching level L to H and the moment the output signal crosses 50% of the rising edge of Q output (t_{PDH}), or delay time between the moment the input signal crosses the switching level H to L and the moment the output signal crosses 50% of the falling edge of Q output (t_{PDL}).
$t_{PD\overline{L}}$ resp $t_{PD\overline{H}}$		Delay time between the moment the input signal crosses the switching level L to H and the moment the output signal crosses 50% of the falling edge of $\overline{Q}$ output ($t_{PD\overline{L}}$), or delay time between the moment the input signal crosses the switching level H to L and the moment the output signal crosses 50% of the rising edge of $\overline{Q}$ output ($t_{PD\overline{H}}$).
t_{PDLH}		Average of t_{PDH} and $t_{PD\overline{L}}$
t_{PDHL}		Average of t_{PDL} and $t_{PD\overline{H}}$
t_{PD}		Average of t_{PDLH} and t_{PDHL}
t_{PDHd} resp t_{PDLd}		Delay time between the moment the input signal crosses the switching level L to H and the zero crossing of the rising edge of the differential output signal (t_{PDHd}), or delay time between the moment the input signal crosses the switching level H to L and the zero crossing of the falling edge of the differential output signal (t_{PDLd}).
$t_{OD-disp}$	Input Overdrive Dispersion	Change in t_{PD} for different overdrive voltages at the input pins.
$t_{SR-disp}$	Input Slew Rate Dispersion	Change in t_{PD} for different slew rates at the input pins.

Symbol	Text	Description
$t_{CM\text{-}disp}$	Input Common Mode Dispersion	Change in t_{PD} for different common mode voltages at the input pins.
Δt_{PDLH} resp Δt_{PDHL}	Q to $\overline{Q}$ Time Skew	Time skew between 50% levels of the rising edge of Q output and the falling edge of $\overline{Q}$ output (Δt_{PDLH}), or time skew between 50% levels of falling edge of Q output and rising edge of $\overline{Q}$ output (Δt_{PDHL}).
Δt_{PD}	Average Q to $\overline{Q}$ Time Skew	Average of t_{PDLH} and t_{PDHL} for L to H and H to L transients.
Δt_{PDd}	Average Diff. Time Skew	Average of t_{PDHd} and t_{PDLd} for L to H and H to L transients.
t_r/t_{rd}	Output Rise Time (20% - 80%)	Time needed for the (single ended or differential) output voltage to change from 20% of its nominal value to 80%.
t_f/t_{fd}	Output Fall Time (20% - 80%)	Time needed for the (single ended or differential) output voltage to change from 80% of its nominal value to 20%.

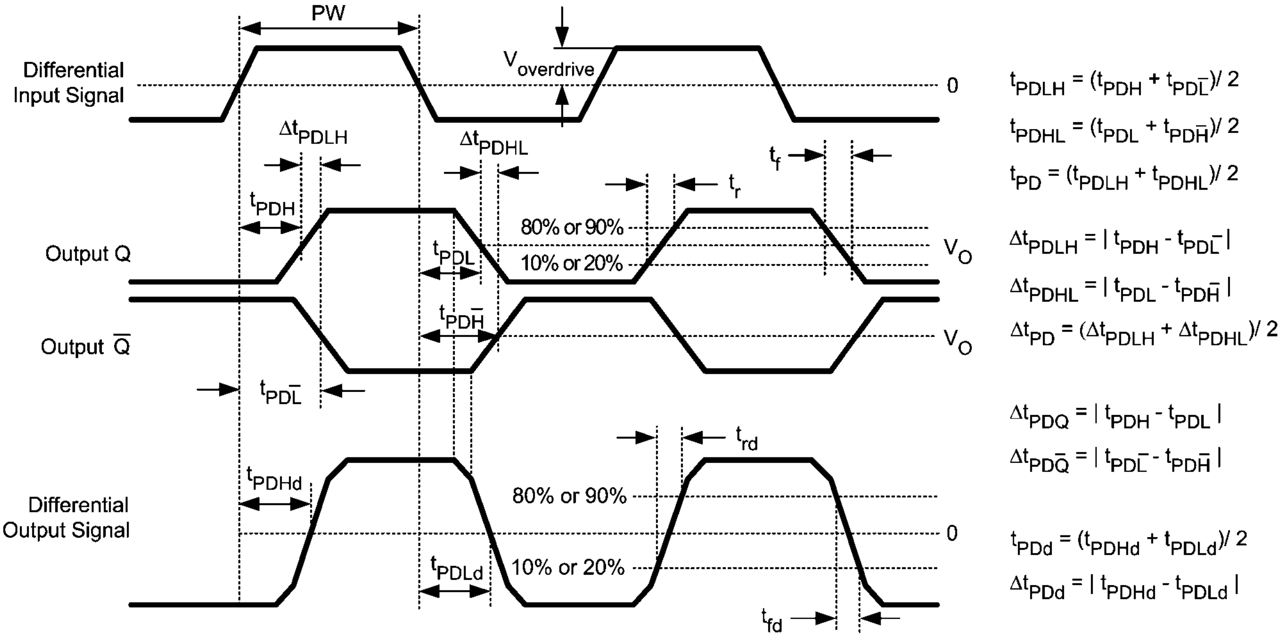

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FIGURE 3. Timing Definitions

PIN DESCRIPTIONS

Pin	Name	Description	Part	Comment
1.	V_{CCO}	Positive Supply Output Stage	A	This supply pin is independent of the supply for the input stage. This allows output levels of different logic families.
2.	$\overline{Q}$	Inverted Output	A	Output levels are determined by the choice of V_{CCOA}.
3.	Q	Output	A	Output levels are determined by the choice of V_{CCOA}.
4.	V_{EE}	Negative Supply	A	All four V_{EE} pins are circular connected together via two antiparallel diodes. (See *Figure 4*)
5.	V_{EE}	Negative Supply	B	All four V_{EE} pins are circular connected together via two antiparallel diodes. (See *Figure 4*)
6.	Q	Output	B	Output levels are determined by the choice of V_{CCOB}.
7.	$\overline{Q}$	Inverted Output	B	Output levels are determined by the choice of V_{CCOB}.
8.	V_{CCO}	Positive Supply Output Stage	B	This supply pin is independent of the supply for the input stage. This allows output levels of different logic families.
9.	V_{CCI}	Positive Supply for Input Stage	B	This supply pin is independent of the supply for the output stage. $V_{CCI}$and V_{CCO} share the same ground pin V_{EE}.

Pin	Name	Description	Part	Comment
10.	IN–	Negative Input	B	Input for analog voltages between 200 mV below V_{EE} and 2V below V_{CCI}.
11.	IN+	Positive Input	B	Input for analog voltages between 200 mV below V_{EE} and 2V below V_{CCI}.
12.	V_{EE}	Negative Supply	B	All four V_{EE} pins are circular connected together via two antiparallel diodes. (See *Figure 4*)
13.	V_{EE}	Negative Supply	C	All four V_{EE} pins are circular connected together via two antiparallel diodes. (See *Figure 4*)
14.	IN+	Positive Input	C	Input for analog voltages between 200 mV below V_{EE} and 2V below V_{CCI}.
15.	IN–	Negative Input	C	Input for analog voltages between 200 mV below V_{EE} and 2V below V_{CCI}.
16.	V_{CCI}	Positive Supply for Input Stage	C	This supply pin is independent of the supply for the output stage. V_{CCI} and V_{CCO} share the same ground pin V_{EE}.
17.	V_{CCO}	Positive Supply Output Stage	C	This supply pin is independent of the supply for the input stage. This allows output levels of different logic families.
18.	$\overline{Q}$	Inverted Output	C	Output levels are determined by the choice of V_{CCOC}.
19.	Q	Output	C	Output levels are determined by the choice of V_{CCOC}.
20.	V_{EE}	Negative Supply	C	All four V_{EE} pins are circular connected together via two antiparallel diodes. (See *Figure 4*)
21.	V_{EE}	Negative Supply	D	All four V_{EE} pins are circular connected together via two antiparallel diodes. (See *Figure 4*)
22.	Q	Output	D	Output levels are determined by the choice of V_{CCOD}.
23.	$\overline{Q}$	Inverted Output	D	Output levels are determined by the choice of V_{CCOD}.
24.	V_{CCO}	Positive Supply Output Stage	D	This supply pin is independent of the supply for the input stage. This allows output levels of different logic families.
25.	V_{CCI}	Positive Supply for Input Stage	D	This supply pin is independent of the supply for the output stage. V_{CCI} and V_{CCO} share the same ground pin V_{EE}.
26.	IN–	Negative Input	D	Input for analog voltages between 200 mV below V_{EE} and 2V below V_{CCI}.
27.	IN+	Positive Input	D	Input for analog voltages between 200 mV below V_{EE} and 2V below V_{CCI}.
28.	V_{EE}	Negative Supply	D	All four V_{EE} pins are circular connected together via two antiparallel diodes. (See *Figure 4*)
29.	V_{EE}	Negative Supply	A	All four V_{EE} pins are circular connected together via two antiparallel diodes. (See *Figure 4*)
30.	IN+	Positive Input	A	Input for analog voltages between 200 mV below V_{EE} and 2V below V_{CCI}.
31.	IN–	Negative Input	A	Input for analog voltages between 200 mV below V_{EE} and 2V below V_{CCI}.
32.	V_{CCI}	Positive Supply for Input Stage	A	This supply pin is independent of the supply for the output stage. V_{CCI} and V_{CCO} share the same ground pin V_{EE}.
33.	DAP	Central Pad at the Bottom of the Package	All	The purpose of this pad is to transfer heat outside the part.

TIPS & TRICKS USING THE LMH7324

This section discusses several aspects concerning special applications using the LMH7324.Topics include the connection of the DAP in conjunction to the V_{EE} pins and the use of this part as an interface between several logic families. Other sections discuss several widely used definitions and terms for comparators. The final sections explain some aspects of transmission lines and the choice for the most suitable components handling very fast pulses.

THE DAP AND THE V_{EE} PINS

To protect the device against damage during handling and production, two antiparallel connected diodes are placed between the V_{EE} pins. Under normal operating conditions (all V_{EE} pins have the same voltage level) these diodes are not functioning, as can be seen in *Figure 4*.

The DAP (Die Attach Paddle) functions as a heat sink which means that heat can be transferred, using vias below this pad, to any appropriate copper plane. The DAP is isolated from all other electrical connections and therefore it is possible to connect this pad to any voltage within the allowed voltage range of the part. Using a DAP connection it is common practice to connect such a pad to the lowest supply voltage. However in high frequency designs it can be useful to connect this pad to another supply such as e.g. the ground plane, while the V_{EE} is for example -5 Volt.

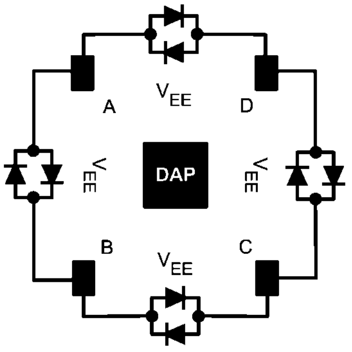

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FIGURE 4. DAP and V_{EE} Configuration

INTERFACE BETWEEN LOGIC FAMILIES

The LMH7324 can be used to interface between different logic families. The feature that facilitates this is the fact that the input stage and the output stage use different positive power supply pins which can be used at different voltages. The only restriction is that both input (V_{CCI}) and output (V_{CCO}) supplies require a minimum of 5V difference relative to V_{EE}. The negative supply pins are connected together for all four parts. Using the power pins at different supply voltages enables level-translation between two logic families. For example, it is possible to translate from logic at negative voltage levels , such as ECL, to logic at positive levels, such as RSPECL and LVDS and vice versa.

Interface from ECL to RSPECL

The supply pin V_{CCI} can be connected to ground because the input levels are negative and V_{EE} is at −5.2V. With this setup the minimum requirements for the supply voltage of 5V are obtained. The V_{CCO} pin must operate at +5V to create the RSPECL levels. (See *Figure 5*.)

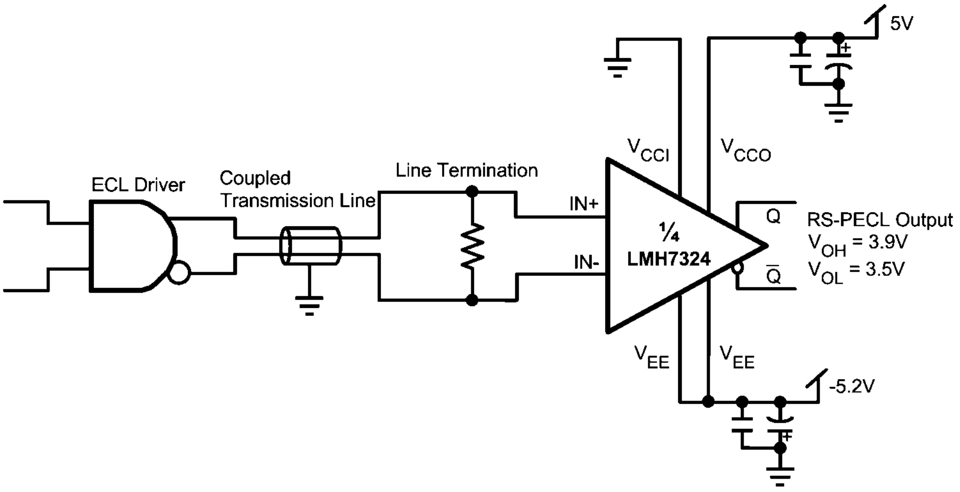

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FIGURE 5. ECL TO RSPECL

Interface from PECL to (RS) ECL

This setup needs the V_{CCI} pin at +5V because the input logic levels are positive. To obtain the ECL levels at the output it is necessary to connect the V_{CCO} to the ground while the V_{EE} has to be connected to the −5.2V. The reason for this is that the minimum requirement for the supply is 5V. The high level of the output of the LMH7324 is normally 1.1V below the V_{CCO} supply voltage, and the low level is 1.5V below this supply. The output levels are now −1100 mV for the logic '1' and −1500 mV for the logic '0'. (See *Figure 6*.)

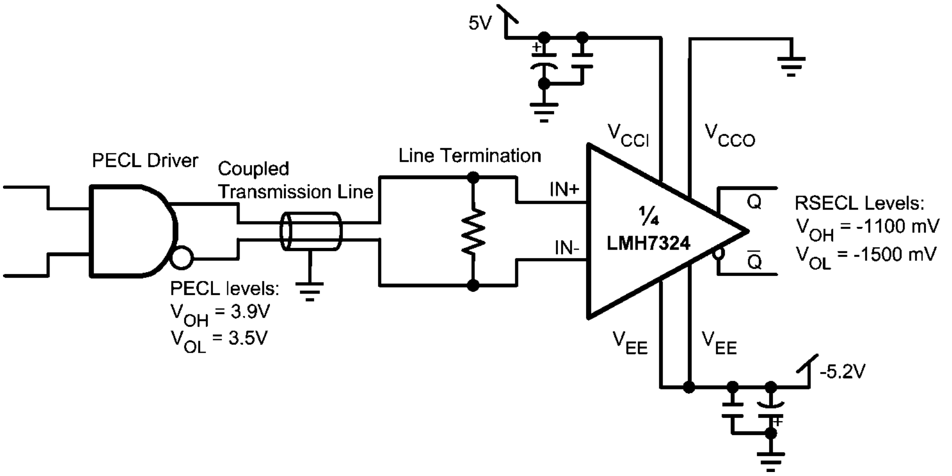

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FIGURE 6. PECL TO RSECL

Interface from Analog to LVDS

As seen in *Figure 7*, the LMH7324 can be configured to create LVDS levels. This is done by connecting the V_{CCO} to 2.5V. As discussed before, the output levels are now at V_{CCO} −1.1V for the logic '1' and at V_{CCO} -1.5V for the logic '0'. These levels of 1000 mV and 1400 mV comply with the LVDS levels. As can be seen in this setup, an AC coupled signal via a transmission line is used. This signal is terminated with 50Ω to the ground. The input stage has its supply from +5V to −5V, which means that the input common mode level is midway between the input stage supply voltages.

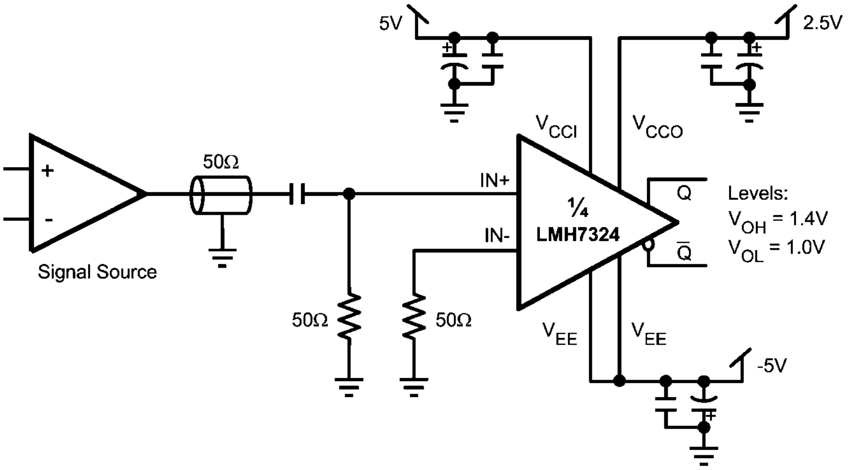

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FIGURE 7. ANALOG TO LVDS

STANDARD COMPARATOR SETUP

Figure 8 shows a standard comparator setup which creates RSPECL levels because the V_{CCO} supply voltage is +5V. In this setup the V_{EE} pin is connected to the ground level. The V_{CCI} pin is connected to the V_{CCO} pin because there is no need to use different positive supply voltages. The input signal is AC coupled to the positive input. To maintain reliable results, even for signals with larger amplitudes, the input pins IN+ and IN− are biased at 1.4V through a resistive divider using a resistor of 1 kΩ to ground and a resistor of 2.5 kΩ to the V_{CC} and by adding two decoupling capacitors. Both inputs are connected to the bias level by the use of a 10 kΩ resistor. With this input configuration the input stage can work in a linear area with signals of approximately 3 V_{PP}. (See input level restrictions in the data tables.)

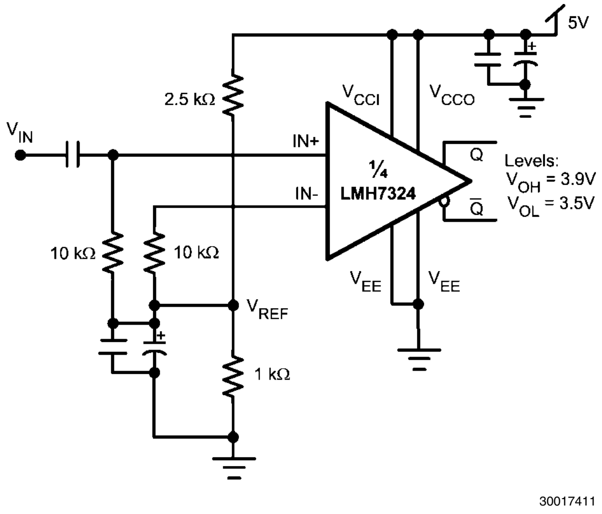

FIGURE 8. Standard Setup

DELAY AND DISPERSION

Comparators are widely used to connect the analog world to the digital one. The accuracy of a comparator is dictated by its DC properties, such as offset voltage and hysteresis, and by its timing aspects, such as rise and fall times and delay. For low frequency applications most comparators are much faster than the analog input signals they handle. The timing aspects are less important here than the accuracy of the input switching levels. The higher the frequencies, the more important the timing properties of the comparator become, because the response of the comparator can make a noticeable change in critical parameters such as time frame or duty cycle. A designer has to know these effects and has to deal with them. In order to predict what the output signal will do, several parameters are defined which describe the behavior of the comparator. For a good understanding of the timing parameters discussed in the following section, a brief explanation is given and several timing diagrams are shown for clarification.

PROPAGATION DELAY

The propagation delay parameter is described in the definition section. Two delay parameters can be distinguished, t_{PDH} and t_{PDL} as shown in *Figure 9*. Both parameters do not necessarily have the same value. It is possible that differences will occur due to a different response of the internal circuitry. As a derivative of this effect another parameter is defined: Δt_{PD}. This parameter is defined as the absolute value of the difference between t_{PDH} and t_{PDL}.

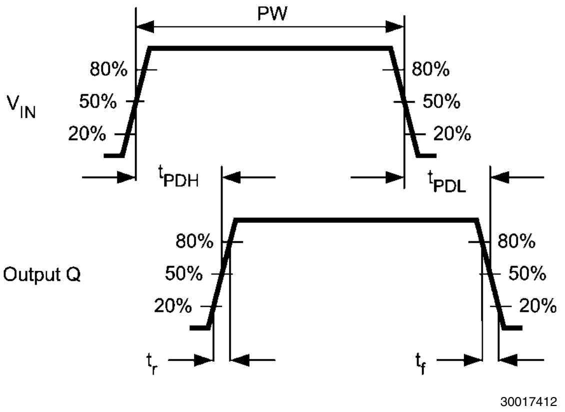

FIGURE 9. Propagation Delay

If Δt_{PD} is not zero, duty cycle distortion will occur. For example when applying a symmetrical waveform (e.g. a sinewave) at the input, it is expected that the comparator will produce a symmetrical square wave at the output with a duty cycle of 50%. When t_{PDH} and t_{PDL} are different, the duty cycle of the output signal will not remain at 50%, but will be increased or decreased. In addition to the propagation delay parameters for single ended outputs discussed before, there are other parameters in the case of complementary outputs. These parameters describe the delay from input to each of the outputs and the difference between both delay times. (See *Figure 10*.) When the differential input signal crosses the reference level from L to H, both outputs will switch to their new state with some delay. This is defined as t_{PDH} for the Q output and $t_{PD\bar{L}}$ for the $\bar{Q}$ output, while the difference between both signals is defined as Δt_{PDLH}. Similar definitions for the falling slope of the input signal can be seen in *Figure 3*.

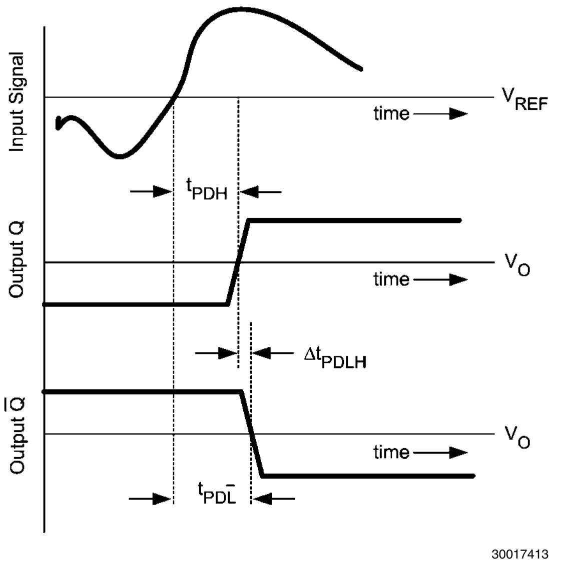

FIGURE 10. t_{PD} with Complementary Outputs

Both output circuits should be symmetrical. At the moment one output is switching ‘on’ the other is switching ‘off’ with ideally no skew between both outputs. The design of the LMH7324 is optimized so that this timing difference is minimized. The propagation delay, t_{PD}, is defined as the average delay of both outputs at both slopes: $(t_{PDLH} + t_{PDHL})/2$. Both overdrive and starting point should be equally divided around the V_{REF} (absolute values).

DISPERSION

There are several circumstances that will produce a variation of the propagation delay time. This effect is called dispersion.

Amplitude Overdrive Dispersion

One of the parameters that causes dispersion is the amplitude variation of the input signal. *Figure 11* shows the dispersion due to a variation of the input overdrive voltage. The overdrive is defined as the 'go to' differential voltage applied to the inputs. *Figure 11* shows the impact it has on the propagation delay time if the overdrive is varied from 10 mV to 100 mV. This parameter is measured with a constant slew rate of the input signal.

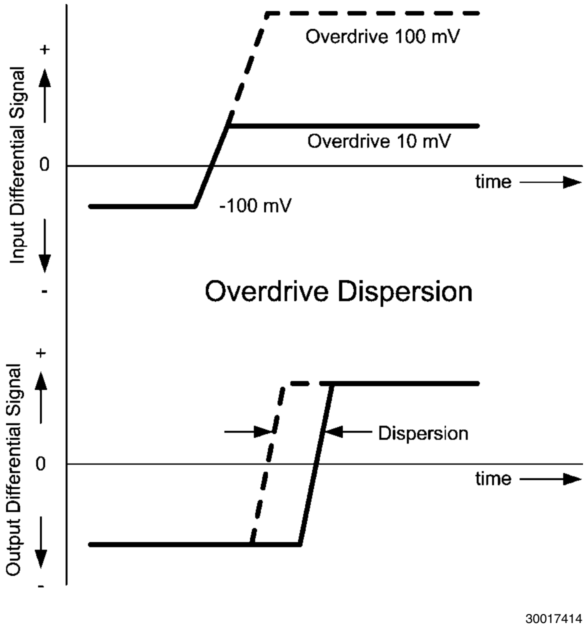

FIGURE 11. Overdrive Dispersion

The overdrive dispersion is caused by the switching currents in the input stage which are dependent on the level of the differential input signal.

Slew Rate Dispersion

The slew rate is another parameter that affects propagation delay. The higher the input slew rate, the faster the input stage switches. (See *Figure 12*.)

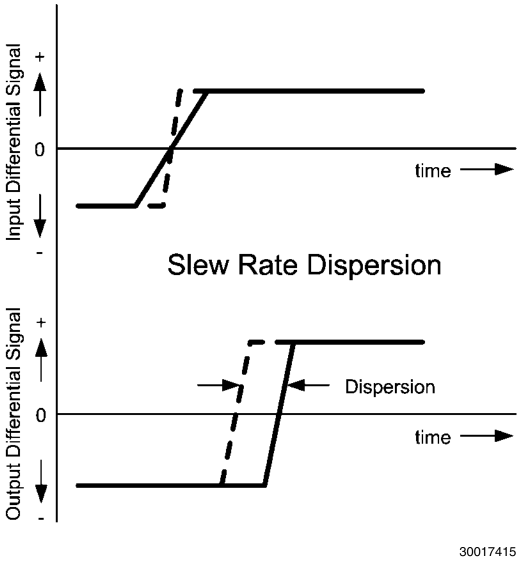

FIGURE 12. Slew Rate Dispersion

A combination of overdrive and slew rate dispersion occurs when applying signals with different amplitudes at constant frequency. A small amplitude will produce a small voltage change per time unit (dV/dt) but also a small maximum switching current (overdrive) in the input transistors. High amplitudes produce a high dV/dt and a bigger overdrive.

Common Mode Dispersion

Dispersion will also occur when changing the common mode level of the input signal. (See *Figure 13*.) When V_{REF} is swept through the CMVR (Common Mode Voltage Range), it results in a variation of the propagation delay time. This variation is called Common Mode Dispersion.

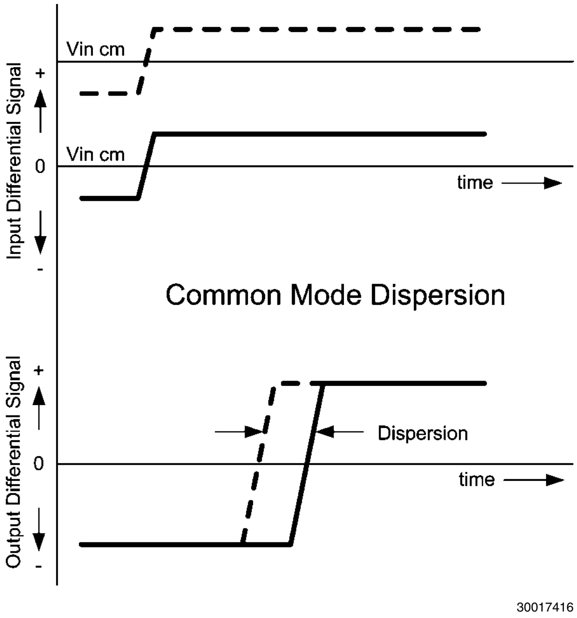

FIGURE 13. Common Mode Dispersion

All of the dispersion effects described previously influence the propagation delay. In practice the dispersion is often caused by a combination of more than one varied parameter.

HYSTERESIS & OSCILLATIONS

In contrast to an op amp, the output of a comparator has only two defined states ‘0’ or ‘1.’ Due to finite comparator gain however, there will be a small band of input differential voltage where the output is in an undefined state. An input signal with fast slopes will pass this band very quickly without problems. During slow slopes however, passing the band of uncertainty can take a relatively long time. This enables the comparators output to switch back and forth several times between ‘0’ and ‘1’ on a single slope. The comparator will switch on its input noise, ground bounce (possible oscillations), ringing etc. Noise in the input signal will also contribute to these undesired switching actions.

The next sections explain these phenomena in situations where no hysteresis is applied, and discuss the possible improvement hysteresis can give.

Using No Hysteresis

Figure 14 shows what happens when the input signal rises from just under the threshold V_{REF} to a level just above it. From the moment the input reaches the lowest dotted line around V_{REF} at t = 0, the output toggles on noise etc. Toggling ends when the input signal leaves the undefined area at t = 1. In this example the output was fast enough to toggle three times. Due to this behavior digital circuitry connected to the output will count a wrong number of pulses. One way to prevent this is to choose a very slow comparator with an output that is not able to switch more than once between ‘0’ and ‘1’ during the time the input state is undefined.

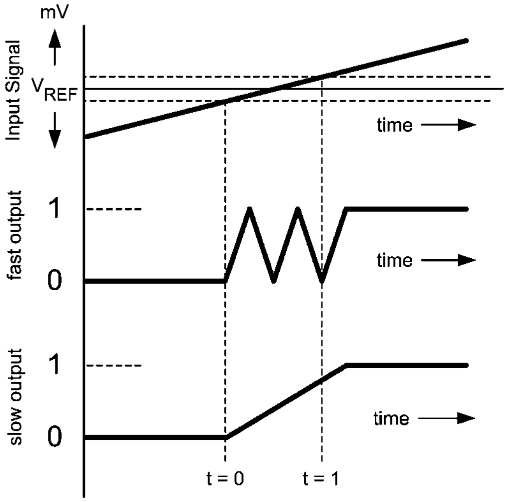

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FIGURE 14. Oscillations on Output Signal

In most circumstances this is not an option because the slew rate of the input signal will vary.

Using Hysteresis

A good way to avoid oscillations and noise during slow slopes is the use of hysteresis. With hysteresis the switching level is forced to a new level at the moment the input signal crosses this level. This can be seen in *Figure 15*.

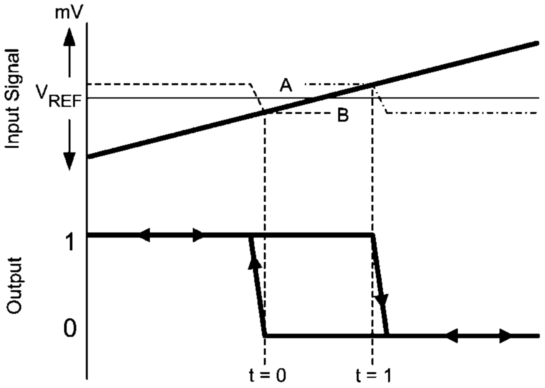

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FIGURE 15. Hysteresis

In this picture there are two dotted lines A and B, both indicating the resulting level at which the comparator output will switch over. Assume that for this situation the input signal is connected to the negative input and the switching level (V_{REF}) to the positive input. The LMH7324 has a built-in hysteresis voltage that is fixed at approximately 20 mV_{PP}. The input level of *Figure 15* starts much lower than the reference level and this means that the state of the input stage is well defined with the inverting input much lower than the non-inverting input. As a result the output will be in the high state. Internally the switching level is at A, with the input signal sloping up, this situation remains until V_{IN} crosses level A at t = 1. Now the output toggles, and the internal switching level is lowered to level B. So before the output has the possibility to toggle again, the difference between the inputs is made sufficient to have a stable situation again. When the input signal comes down from high to low, the situation is stable until level B is reached at t = 0. At this moment the output will toggle back, and the circuit is back in the starting situation with the inverting input at a much lower level than the non-inverting input. In the situation without hysteresis, the output will toggle exactly at V_{REF}. With hysteresis this happens at the internally introduced levels A and B, as can be seen in *Figure 15*. If the levels A and B change, due to a change in the built-in hysteresis voltage depending of e.g. temperature variations, then the timing of t = 0 and t = 1 will also vary. The variation of the hysteresis voltage over temperature is very low and ranges from 22 mV to 23 mV at 5V Supply over a temperature variation of -25 °C to 125 °C (see fig *Figure 16*). When designing a circuit be aware of this effect. Introducing hysteresis will cause some time shift between output and input (e.g. duty cycle variations), but will eliminate undesired switching of the output.

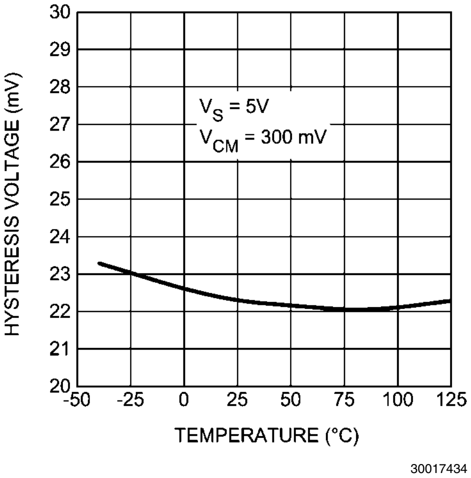


FIGURE 16. Hysteresis Voltage over Temperature

THE OUTPUT

Output Swing Properties

The LMH7324 has differential outputs, which means that both outputs have the same swing but in opposite directions. (See *Figure 17*.) Both outputs swing around the common mode output voltage (V_O). This voltage can be measured at the midpoint between two equal resistors connected to each output. The absolute value of the difference between both voltages is called V_{OD}. The outputs cannot be held at the V_O level because of their digital nature. They only cross this level during a transition. Due to the symmetrical structure of the circuit, both output voltages cross at V_O regardless of whether the output changes from ‘0’ to ‘1’ or vise versa.

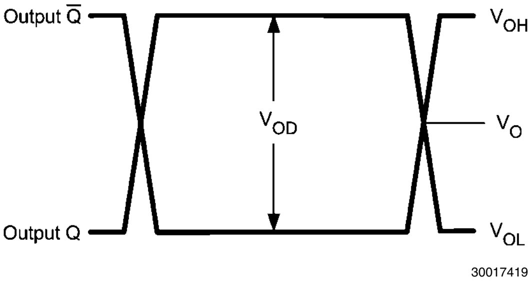


FIGURE 17. Output Swing

Loading the Output

Both outputs are activated when current is flowing through a resistor that is externally connected to V_T. The termination voltage should be set 2V below the V_{CCO}. This makes it possible to terminate each of the outputs directly with 50Ω, and if needed to connect through a transmission line with the same impedance. (See *Figure 18*.) Due to the low ohmic nature of the output emitter followers and the 50Ω load resistor, a capacitive load of several pF does not dramatically affect the speed and shape of the signal. When transmitting the signal from one output to any input the termination resistor should match the transmission line. The capacitive load (C_P) will distort the received signal. When measuring this input with a probe, a certain amount of capacitance from the probe is parallel to the termination resistor. The total capacitance can be as large as 10 pF. In this case there is a pole at:

$f = 1/(2*\pi*C*R)$

$f = 1e9/\pi$

$f = 318$ MHz

For this frequency the current I_P has the same value as the current through the termination resistor. This means that the voltage drops at the input and the rise and fall times are dramatically different from the specified numbers for this part.

Another parasitic capacity that can affect the output signal is the capacity directly between both outputs, called C_{PAR}. (See *Figure 18*.) The LMH7324 has two complementary outputs so there is the possibility that the output signal will be transported by a symmetrical transmission line. In this case both output tracks form a coupled line with their own parasitics and both receiver inputs are connected to the transmission line. Actually the line termination looks like 100Ω and the input capacities, which are in series, are parallel to the 100Ω termination. The best way to measure the input signal is to use a differential probe directly across both inputs. Such a probe is very suitable for measuring these fast signals because it has good high frequency characteristics and low parasitic capacitance.

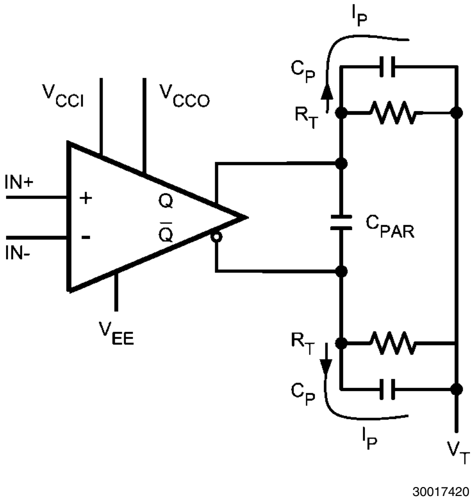


FIGURE 18. Parasitic Capacities

TRANSMISSION LINES & TERMINATION TECHNOLOGIES

The LMH7324 uses complementary RSPECL outputs and emitter followers, which means high output current capability and low sensitivity to parasitic capacitance. The use of Reduced Swing Positive Emitter Coupled Logic gives advantages concerning speed and supply. Data rates are growing, which requires increasing speed. Data is not only connected to other IC’s on a single PCB board but, in many cases, there are interconnections from board to board or from equipment to equipment. Distances can be short or long but it is always necessary to have a reliable connection, which consumes low power and is able to handle high data rates. The complementary outputs of the LMH7324 make it possible to use symmetrical transmission lines. The advantage over single ended signal transmission is that the LMH7324 has higher immunity to common mode noise. Common mode signals are signals that are equally apparent on both lines and because the receiver only looks at the difference between both lines, this noise is canceled.

Maximum Bit Rates

The maximum toggle rate is defined at an amplitude of 50% of the nominal output signal. This toggle rate is a number for the maximum transfer rate of the part and can be given in Hz or in Bps. When transmitting signals in a NRZ (**N**on **R**eturn to **Z**ero) format the bitrate is double this frequency number, because during one period two bits can be transmitted. (See *Figure 19*.) The rise and fall times are very important specifications in high speed circuits. In fact these times determine the maximum toggle rate of the part. Rise and fall times are normally specified at 20% and 80% of the signal amplitude (60% difference). Assuming that the edges at 50% amplitude are coming up and down like a sawtooth it is possible to calculate the maximum toggle rate but this number is too optimistic. In practice the edges are not linear while the pulse shape is more or less a sinewave.

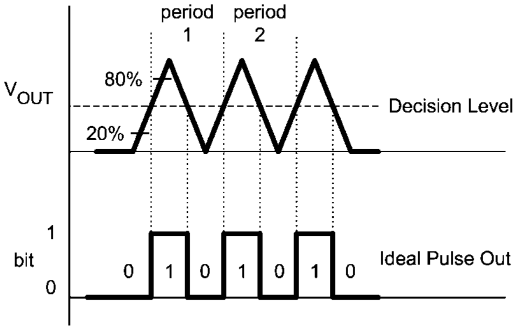


FIGURE 19. Bit Rates

Need for Terminated Transmission Lines

During the 1980’s and 90’s, National fabricated the 100K ECL logic family. The rise and fall time specifications were 0.75 ns, which were considered very fast. If sufficient care has not been given in designing the transmission lines and choosing the correct terminations, then errors in digital circuits are introduced. To be helpful to designers that use ECL with “old” PCB-techniques, the 10K ECL family was introduced with rise and fall time specifications of 2 ns. This is much slower and easier to use. The RSPECL output signals of the LMH7324 have transition times that extend the fastest ECL family. A careful PCB design is needed using RF techniques for transmission and termination.

Transmission lines can be formed in several ways. The most commonly used types are the coaxial cable and the twisted pair telephony cable. (See *Figure 20*.)

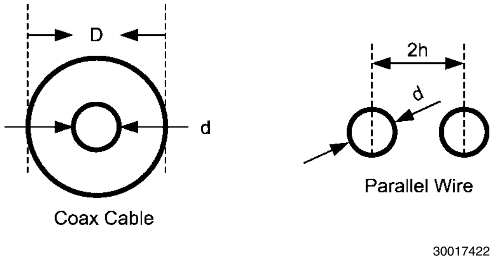


FIGURE 20. Cable Types

These cables have a characteristic impedance determined by their geometric parameters. Widely used impedances for the coaxial cable are 50Ω and 75Ω. Twisted pair cables have impedances of about 120Ω to 150Ω.

Other types of transmission lines are the strip line and the microstrip line. These last types are used on PCB boards. They have the characteristic impedance dictated by the physical dimensions of a track placed over a metal ground plane. (See *Figure 21*.)

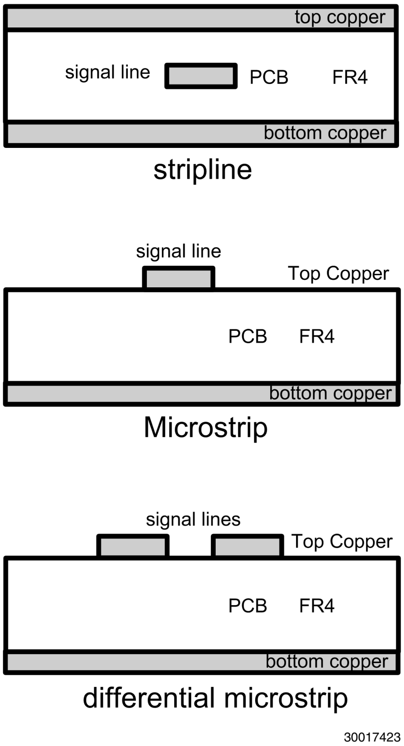


FIGURE 21. PCB Lines

Differential Microstrip Line

The transmission line which is ideally suited for complementary signals is the differential microstrip line. This is a double microstrip line with a narrow space in between. This means both lines have strong coupling and this determines the characteristic impedance. The fact that they are routed above a copper plane does not affect differential impedance, only CM-capacitance is added. Each of the structures above has its own geometric parameters, so for each structure there is a different formula to calculate the right impedance. For calculations on these transmission lines visit the National website or order RAPIDESIGNER. At the end of the transmission line there must be a termination having the same impedance as that of the transmission line itself. It does not matter what impedance the line has, if the load has the same value no reflections will occur. When designing a PCB board with transmission lines on it, space becomes an important item especially on high density boards. With a single microstrip line, line width is fixed for a given impedance and for a specific board material. Other line widths will result in different impedances.

Advantages of Differential Microstrip Lines

Impedances of transmission lines are always dictated by their geometric parameters. This is also true for differential microstrip lines. Using this type of transmission line, the distance of the track determines the resulting impedance. So, if the PCB manufacturer can produce reliable boards with low track spacing the track width for a given impedance is also small. The wider the spacing, the wider tracks are needed for a specific impedance. For example two tracks of 0.2 mm width and 0.1 mm spacing have the same impedance as two tracks of

0.8 mm width and 0.4 mm spacing. With high-end PCB processes, it is possible to design very narrow differential microstrip transmission lines. It is desirable to use these to create optimal connections to the receiving part or the terminating resistor, in accordance to their physical dimensions. Seen from the comparator, the termination resistor must be connected at the far end of the line. Open connections after the termination resistor (e.g. to the input of a receiver) must be as short as possible. The allowed length of such connections varies with the received transients. The faster the transients, the shorter the open lines must be to prevent signal degradation.

PCB LAYOUT CONSIDERATIONS AND COMPONENT VALUE SELECTION

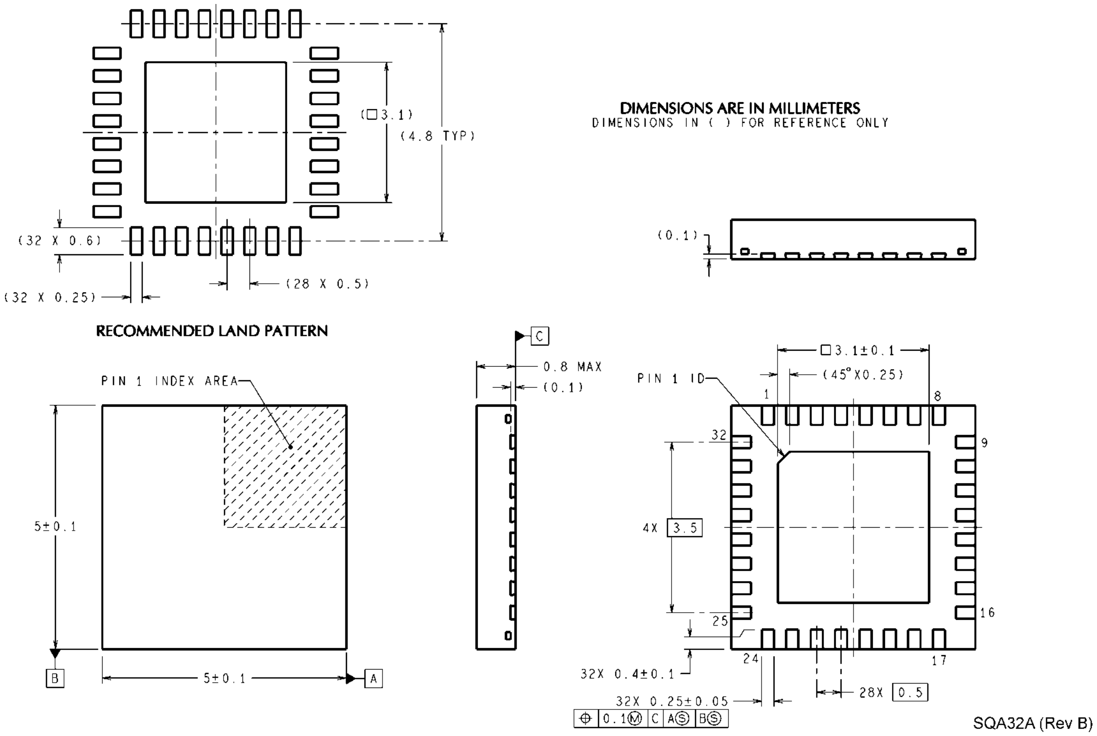
High frequency designs require that both active and passive components be selected from those that are specially designed for this purpose. The LMH7324 is fabricated in a 32-pin LLP package intended for surface mount design. For reliable high speed design it is highly recommended to use small surface mount passive components because these packages have low parasitic capacitance and low inductance simply because they have no leads to connect them to the PCB. It is possible to amplify signals at frequencies of several hundreds of MHz using standard through-hole resistors. Surface mount devices however, are better suited for this purpose. Another important issue is the PCB itself, which is no longer a simple carrier for all the parts and a medium to interconnect them. The PCB becomes a real component itself and consequently contributes its own high frequency properties to the overall performance of the circuit. Good practice dictates that a high frequency design have at least one ground plane, providing a low impedance path for all decoupling capacitors and other ground connections. Care should be given especially that on-board transmission lines have the same impedance as the cables to which they are connected. Most single ended applications have 50Ω impedance (75Ω for video and cable TV applications). Such low impedance, single ended microstrip transmission lines usually require much wider traces (2 to 3 mm) on a standard double sided PCB board than needed for a ‘normal’ trace. Another important issue is that inputs and outputs should not ‘see’ each other. This occurs if input and output tracks are routed in parallel over the PCB with only a small amount of physical separation, particularly when the difference in signal level is high. Furthermore components should be placed as flat and low as possible on the surface of the PCB. For higher frequencies a long lead can act as a coil, a capacitor or an antenna. A pair of leads can even form a transformer. Careful design of the PCB minimizes oscillations, ringing and other unwanted behavior. For ultra high frequency designs only surface mount components will give acceptable results. (For more information see OA-15).

National suggests the following evaluation board as a guide for high frequency layout and as an aid in device testing:

Device	Package	Evaluation Board Ordering ID
LMH7324	SQA32A	LMH7324EVAL

This evaluation board can be shipped when a device sample request is placed with National Semiconductor.

Physical Dimensions inches (millimeters) unless otherwise noted



32-Pin LLP
NS Package Number SQA32A

Notes

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LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
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