

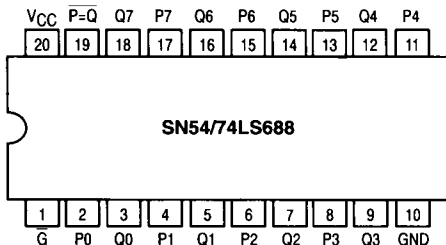
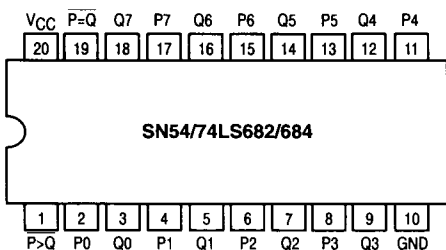


8-BIT MAGNITUDE COMPARATORS

The SN54/74LS682, 684, 688 are 8-bit magnitude comparators. These device types are designed to perform comparisons between two eight-bit binary or BCD words. All device types provide $\overline{P=Q}$ outputs and the LS682 and LS684 have $P>Q$ outputs also.

The LS682, LS684 and LS688 are totem pole devices. The LS682 has a 20 kΩ pullup resistor on the Q inputs for analog or switch data.

CONNECTION DIAGRAMS (TOP VIEW)

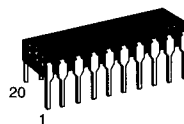


TYPE	$\overline{P=Q}$	$\overline{P>Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	PULLUP
LS682	yes	yes	no	totem-pole	yes
LS684	yes	yes	no	totem-pole	no
LS688	yes	no	yes	totem-pole	no

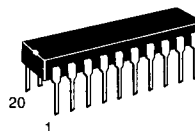
**SN54/74LS682
SN54/74LS684
SN54/74LS688**

8-BIT MAGNITUDE COMPARATORS

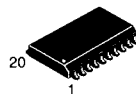
LOW POWER SCHOTTKY



**J SUFFIX
CERAMIC
CASE 732-03**



**N SUFFIX
PLASTIC
CASE 738-03**



**DW SUFFIX
SOIC
CASE 751D-03**

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES		$\overline{P=Q}$	$\overline{P>Q}$
P, Q	$\overline{G}, \overline{GT}$	$\overline{G2}$		
P = Q	L	L	L	H
P > Q	L	L	H	L
P < Q	L	L	H	H
X	H	H	H	H

H = HIGH Level, L = LOW Level, X = Irrelevant

SN54/74LS682 • SN54/74LS684 • SN54/74LS688

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

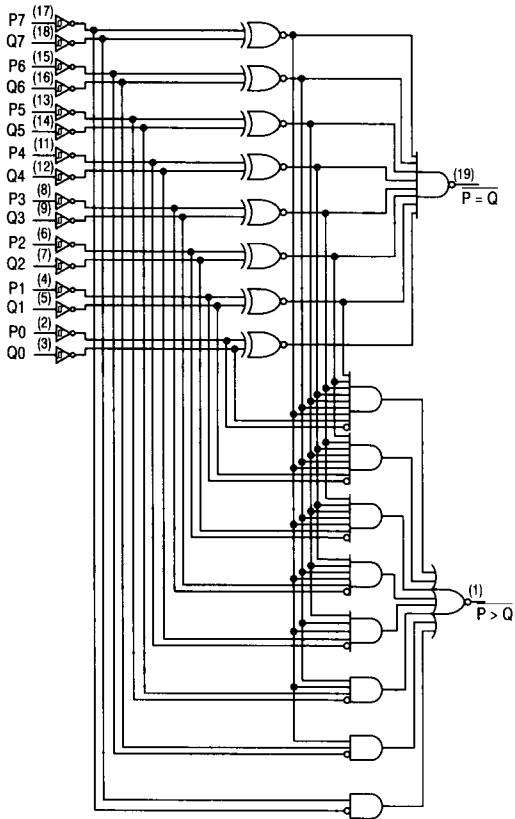
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA
		74		0.35	0.5	V	I _{OL} = 24 mA
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		LS628-Q Inputs			0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V
		Others			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	LS682-Q Inputs			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
		Others			-0.2	mA	
I _{OS}	Short Circuit Current (Note 1)		-30		-130	mA	V _{CC} = MAX
I _{CC}	Power Supply Current	LS682			70	mA	V _{CC} = MAX
		LS684			65	mA	
		LS688			65	mA	

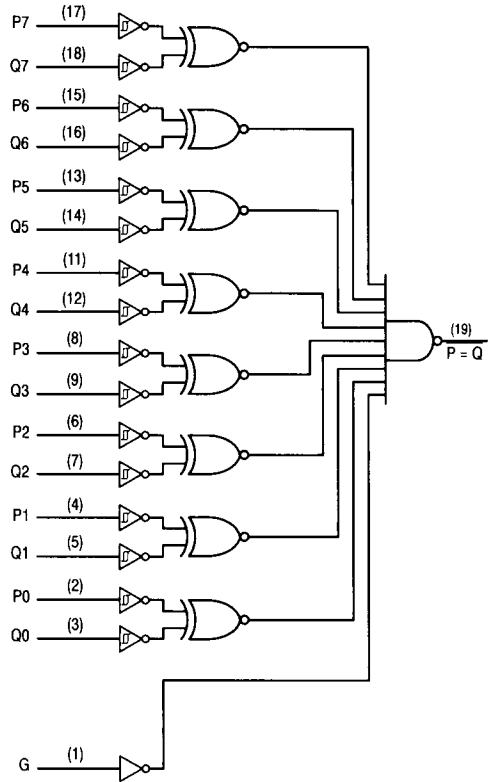
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS682 • SN54/74LS684 • SN54/74LS688

LOGIC DIAGRAMS



SN54/74LS682 thru LS684



SN54/74LS688

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SN54/74LS682•SN54/74LS684•SN54/74LS688

AC CHARACTERISTICS (T_A = 25°C)

SN54/74LS682

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		13 15	25 25	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		14 15	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} > \overline{Q}$		20 15	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} > \overline{Q}$		21 19	30 30	ns	

SN54/74LS684

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		15 17	25 25	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		16 15	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} > \overline{Q}$		22 17	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} > \overline{Q}$		24 20	30 30	ns	

SN54/74LS688

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		12 17	18 23	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		12 17	18 23	ns	
t _{PLH} t _{PHL}	Propagation Delay, \overline{G} , $\overline{G1}$ to $\overline{P} = \overline{Q}$		12 13	18 20	ns	