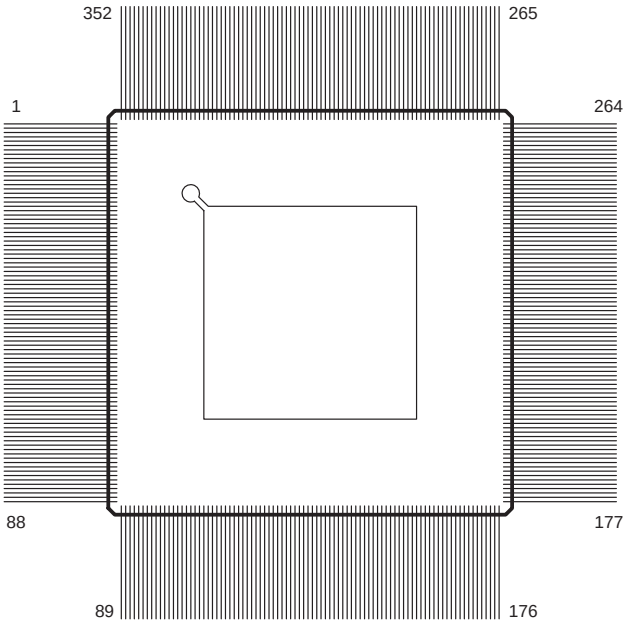
- **Performance**
  - **40 MFLOPS (Million Floating-Point Operations per Second) With 256-Megabyte/s Burst I/O Rate for 40-MHz Modules**
  - **128K Word × 32 Bit Zero-Wait-State SRAM Connected to the ’C40 Local Bus**
- **Compliant to MIL-PRF-38535 QML**
- **’C40 Performance With Local Memory Requiring Only 4.35 Square Inches of Board Space**
- **Enhanced Performance Offered By Multichip-Module Solution**
  - **46% Reduction In Number of Interconnects**
  - **23% Reduction (Minimum) in Board Area**
  - **Estimated 20% Reduction in Power Dissipation Due to Reduced Parasitic Capacitance and Interconnect Lengths**
- **Two Memory Ports for High Data Bandwidth**
  - **Full 2-Gigaword External Bus**
  - **Internal Bus Mapped to 128K Word × 32 Bit Zero-Wait-State SRAM**
- **Six External Communication Ports for Direct Processor-to-Processor Communication**
- **Supports IEEE-1149.1† -Compliant (JTAG) With Boundary-Scan Testing**
- **Operating Free-Air Temperature Ranges:**
  - **Military: –55°C to 125°C**
  - **Commercial: 0°C to 70°C**
- **Packaging:**
  352-Lead Ceramic Quad Flatpack
  (HFH Suffix)

352-LEAD HFH QUAD FLATPACK PACKAGE
(TOP VIEW)



ADVANCE INFORMATION

description

The ’MCM41 single-SMJ320C40 multichip module‡ (MCM) contains one SMJ320C40 device with 128K word × 32 bit zero-wait-state SRAM mapped to the local memory bus. The MCM is footprint-compatible with the monolithic ’320C40HFH package to allow easy upgradeability and design-in. The local memory bus is not routed to the device footprint. The ’MCM41 is available in both a commercial temperature range (0°C to 70°C) and a military temperature range (–55°C to 125°C) option.

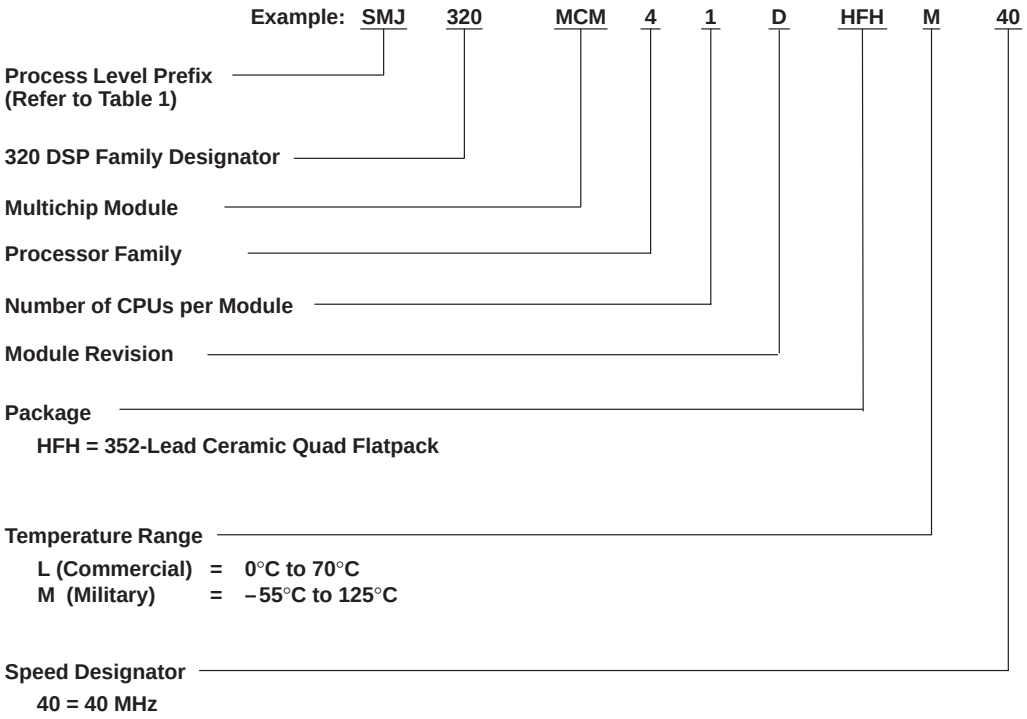
†IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture
‡The ’MCM41 single-SMJ320C40 multichip module will be referred to as ’MCM41 throughout this data sheet.

Table 1. MCM Processing Matrix

PROCESS LEVEL	TEMPERATURE RANGE		DIE	100% PROCESSED	SPEED TEST	TEST TEMPERATURE RANGE	QUALIFICATION TESTING
SM	L version	0°C to 70°C	Probed	No	No	25°C to 70°C	Package
	M version	–55°C to 125°C	Probed	No	Yes	–55°C to 125°C	Package
SMJ†	M version	–55°C to 125°C	KGD‡	Yes	Yes	–55°C to 125°C	MIL-H-38534

† SMJ-level product is fully MIL-PRF-38535 QML compliant.
‡ KGD stands for the known-good-die strategy as defined in the reference documentation and data sheet scope section.

Multichip Module Naming Nomenclature and Ordering Information



For descriptions of the HFH package pin assignments, refer to the SMJ320C40 signals descriptions table in the SMJ320C40 data sheet (literature number SGUS017).

ADVANCE INFORMATION

HFH package pin assignments — numerical listing

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
01	D31	41	D0	81	$\overline{\text{CSTRB5}}$	121	DV_{DD}‡	161	C1D7
02	D30	42	$\overline{\text{CE1}}$	82	$\overline{\text{CACK5}}$	122	IV_{SS}†	162	C1D6
03	D29	43	$\overline{\text{RDY1}}$	83	$\overline{\text{CREQ5}}$	123	IV_{SS}†	163	C1D5
04	D28	44	DV_{SS}§	84	$\overline{\text{CRDY4}}$	124	C2D7	164	C1D4
05	D27	45	DV_{SS}§	85	$\overline{\text{CSTRB4}}$	125	C2D6	165	C1D3
06	D26	46	CV_{SS}†	86	$\overline{\text{CACK4}}$	126	C2D5	166	C1D2
07	$GDDV_{DD}$‡	47	CV_{SS}†	87	$\overline{\text{CREQ4}}$	127	C2D4	167	C1D1
08	D25	48	$\overline{\text{LOCK}}$	88	CV_{SS}†	128	C2D3	168	C1D0
09	D24	49	V_{DDL}¶	89	DV_{SS}§	129	C2D2	169	DV_{DD}‡
10	D23	50	V_{SSL}#	90	DV_{SS}§	130	C2D1	170	C0D7
11	D22	51	$\overline{\text{CE0}}$	91	DV_{DD}‡	131	C2D0	171	C0D6
12	D21	52	$\overline{\text{RDY0}}$	92	C5D7	132	CV_{SS}†	172	C0D5
13	D20	53	$\overline{\text{DE}}$	93	C5D6	133	DV_{SS}§	173	C0D4
14	D19	54	TCK	94	C5D5	134	DV_{SS}§	174	C0D3
15	D18	55	TDO	95	C5D4	135	DV_{DD}‡	175	C0D2
16	D17	56	TDI	96	C5D3	136	$\overline{\text{CRDY3}}$	176	C0D1
17	D16	57	TMS	97	C5D2	137	$\overline{\text{CSTRB3}}$	177	C0D0
18	CV_{SS}†	58	$\overline{\text{TRST}}$	98	C5D1	138	$\overline{\text{CACK3}}$	178	CV_{SS}†
19	CV_{SS}†	59	EMU0	99	C5D0	139	$\overline{\text{CREQ3}}$	179	DV_{DD}‡
20	IV_{SS}†	60	EMU1	100	DV_{DD}‡	140	V_{DDL}¶	180	ROMEN
21	$GDDV_{DD}$‡	61	DV_{SS}§	101	C4D7	141	V_{SSL}#	181	$\overline{\text{IIOF0}}$
22	$GDDV_{DD}$‡	62	DV_{SS}§	102	C4D6	142	$\overline{\text{CRDY2}}$	182	DV_{SS}§
23	DV_{SS}§	63	DV_{DD}‡	103	C4D5	143	$\overline{\text{CSTRB2}}$	183	DV_{SS}§
24	DV_{SS}§	64	PAGE1	104	C4D4	144	$\overline{\text{CACK2}}$	184	$\overline{\text{IIOF1}}$
25	D15	65	R/$\overline{\text{W}}$1	105	C4D3	145	$\overline{\text{CREQ2}}$	185	$\overline{\text{IIOF2}}$
26	D14	66	$\overline{\text{STRB1}}$	106	C4D2	146	DV_{DD}‡	186	$\overline{\text{IIOF3}}$
27	D13	67	STAT0	107	C4D1	147	$\overline{\text{CRDY1}}$	187	$\overline{\text{NMI}}$
28	D12	68	STAT1	108	C4D0	148	$\overline{\text{CSTRB1}}$	188	NC‖
29	D11	69	IV_{SS}†	109	CV_{SS}†	149	$\overline{\text{CACK1}}$	189	NC‖
30	D10	70	STAT2	110	DV_{SS}§	150	$\overline{\text{CREQ1}}$	190	NC‖
31	D9	71	STAT3	111	DV_{SS}§	151	$\overline{\text{CRDY0}}$	191	NC‖
32	D8	72	PAGE0	112	DV_{DD}‡	152	$\overline{\text{CSTRB0}}$	192	NC‖
33	D7	73	R/$\overline{\text{W}}$0	113	C3D7	153	$\overline{\text{CACK0}}$	193	NC‖
34	D6	74	$\overline{\text{STRB0}}$	114	C3D6	154	$\overline{\text{CREQ0}}$	194	NC‖
35	D5	75	$\overline{\text{AE}}$	115	C3D5	155	CV_{SS}†	195	DV_{DD}‡
36	$GDDV_{DD}$‡	76	RESETLOC1	116	C3D4	156	CV_{SS}†	196	CV_{SS}†
37	D4	77	DV_{DD}‡	117	C3D3	157	DV_{SS}§	197	NC‖
38	D3	78	RESETLOC0	118	C3D2	158	DV_{SS}§	198	NC‖
39	D2	79	$\overline{\text{RESET}}$	119	C3D1	159	IV_{SS}†	199	NC‖
40	D1	80	$\overline{\text{CRDY5}}$	120	C3D0	160	DV_{DD}‡	200	NC‖

† CV_{SS} and IV_{SS} pins are connected internally.
‡ DV_{DD}, $LADV_{DD}$, $LDDV_{DD}$, $GDDV_{DD}$, and $GADV_{DD}$ pins are connected internally.
§ DV_{SS} pins are connected internally.
¶ V_{DDL} pins are connected internally.
# V_{SSL} pins are connected internally.
‖ Pins marked NC should be left electrically unconnected.

ADVANCE INFORMATION

HFH package pin assignments — numerical listing (continued)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
201	TCLK0	241	CV_{SS}†	281	$LDDV_{DD}$‡	321	A20
202	TCLK1	242	DV_{SS}§	282	CV_{SS}†	322	A19
203	H3	243	DV_{SS}§	283	DV_{SS}§	323	A18
204	H1	244	NC‖	284	DV_{SS}§	324	A17
205	NC‖	245	NC‖	285	IV_{SS}†	325	$GADV_{DD}$‡
206	IV_{SS}†	246	NC‖	286	NC‖	326	$GADV_{DD}$‡
207	NC‖	247	NC‖	287	NC‖	327	CV_{SS}†
208	NC‖	248	NC‖	288	NC‖	328	CV_{SS}†
209	NC‖	249	NC‖	289	NC‖	329	DV_{SS}§
210	NC‖	250	NC‖	290	NC‖	330	DV_{SS}§
211	NC‖	251	NC‖	291	NC‖	331	A16
212	$\overline{IACK}$	252	NC‖	292	NC‖	332	A15
213	V_{DDL}¶	253	NC‖	293	NC‖	333	A14
214	V_{SSL}#	254	NC‖	294	NC‖	334	A13
215	X1	255	NC‖	295	NC‖	335	A12
216	X2/CLKIN	256	$LADV_{DD}$‡	296	NC‖	336	A11
217	CV_{SS}†	257	NC‖	297	NC‖	337	A10
218	CV_{SS}†	258	NC‖	298	$LDDV_{DD}$‡	338	A9
219	DV_{DD}‡	259	NC‖	299	NC‖	339	A8
220	DV_{SS}§	260	NC‖	300	NC‖	340	A7
221	DV_{SS}§	261	DV_{SS}§	301	NC‖	341	A6
222	NC‖	262	DV_{SS}§	302	NC‖	342	A5
223	NC‖	263	CV_{SS}†	303	NC‖	343	A4
224	NC‖	264	NC‖	304	V_{DDL}¶	344	$GADV_{DD}$‡
225	NC‖	265	NC‖	305	V_{SSL}#	345	A3
226	$LADV_{DD}$‡	266	NC‖	306	CV_{SS}†	346	A2
227	NC‖	267	NC‖	307	CV_{SS}†	347	A1
228	NC‖	268	$LDDV_{DD}$‡	308	DV_{SS}§	348	A0
229	NC‖	269	NC‖	309	DV_{SS}§	349	CV_{SS}†
230	NC‖	270	NC‖	310	A30	350	DV_{SS}§
231	NC‖	271	NC‖	311	A29	351	DV_{SS}§
232	NC‖	272	NC‖	312	A28	352	SUBS
233	NC‖	273	NC‖	313	$GADV_{DD}$‡		
234	NC‖	274	NC‖	314	A27		
235	NC‖	275	NC‖	315	A26		
236	NC‖	276	NC‖	316	A25		
237	NC‖	277	NC‖	317	A24		
238	$LADV_{DD}$‡	278	NC‖	318	A23		
239	$LADV_{DD}$‡	279	NC‖	319	A22		
240	CV_{SS}†	280	$LDDV_{DD}$‡	320	A21		

† CV_{SS} and IV_{SS} pins are connected internally.
‡ DV_{DD}, $LADV_{DD}$, $LDDV_{DD}$, $GDDV_{DD}$, and $GADV_{DD}$ pins are connected internally.
§ DV_{SS} pins are connected internally.
¶ V_{DDL} pins are connected internally.
# V_{SSL} pins are connected internally.
‖ Pins marked NC should be left electrically unconnected.

ADVANCE INFORMATION

functional block diagram

The following pins have 10-kΩ pullup resistors added within the module:

- $\overline{\text{CREQx}}$, $\overline{\text{CACKx}}$, $\overline{\text{CSTRBx}}$, $\overline{\text{CRDYx}}$, where x = 0–5
- $\overline{\text{LCE1}}$ (internal connections)

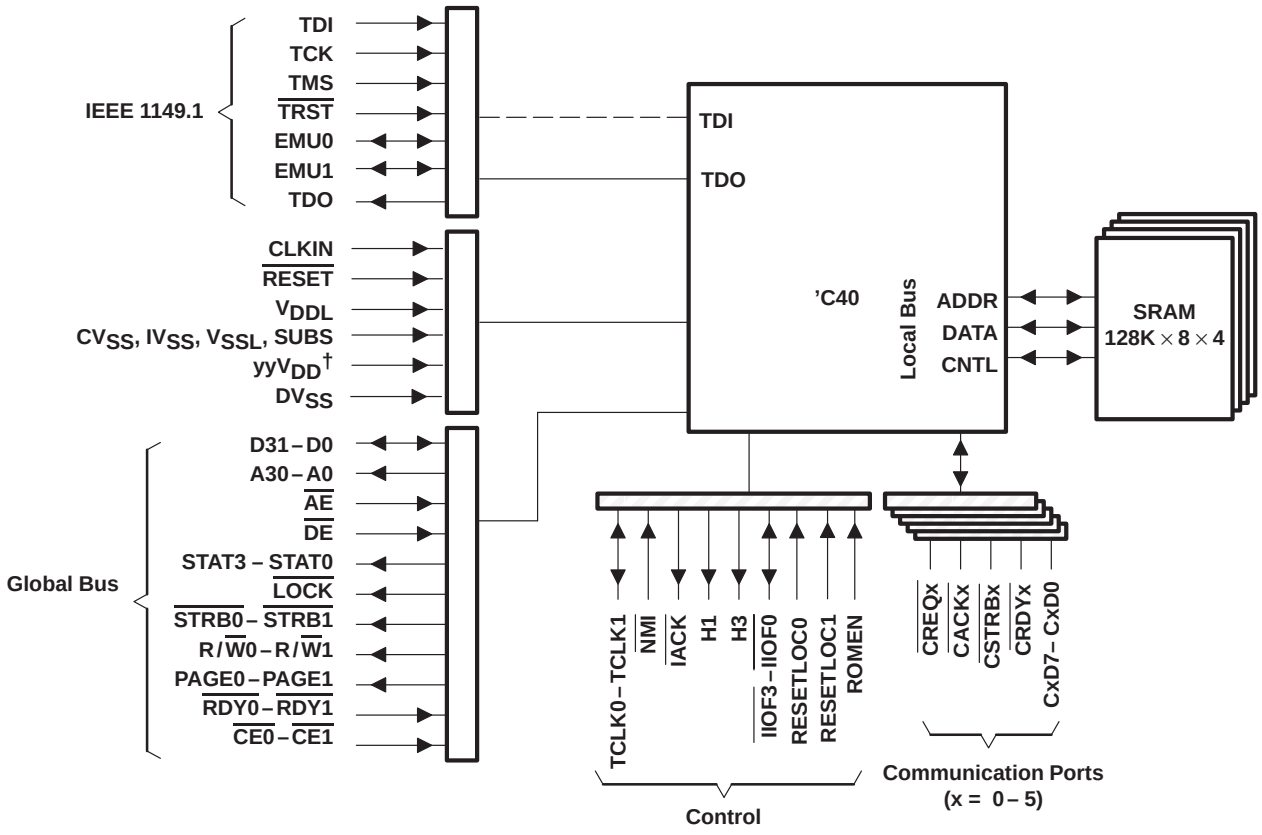
A total of eight decoupling capacitors have been connected within the module.

Between clean power and ground (V_{DDL} and CV_{SS}), the following capacitors have been connected:

- One 0.1-µF capacitor
- One 0.01-µF capacitor

Between dirty power and ground ($GDDV_{DD}$, $GADV_{DD}$, $LDDV_{DD}$, $LADV_{DD}$, and DV_{SS}), the following capacitors have been connected:

- Three 0.1-µF capacitors
- Three 0.01-µF capacitors



† yyV_{DD} represents $GDDV_{DD}$, $GADV_{DD}$, $LDDV_{DD}$, and $LADV_{DD}$.

operational overview

Treatment of the detailed operation of the 'C40 device is beyond the scope of this document. Refer to the *TMS320C4x User's Guide* (literature number SPRU063) for a detailed description of this DSP.

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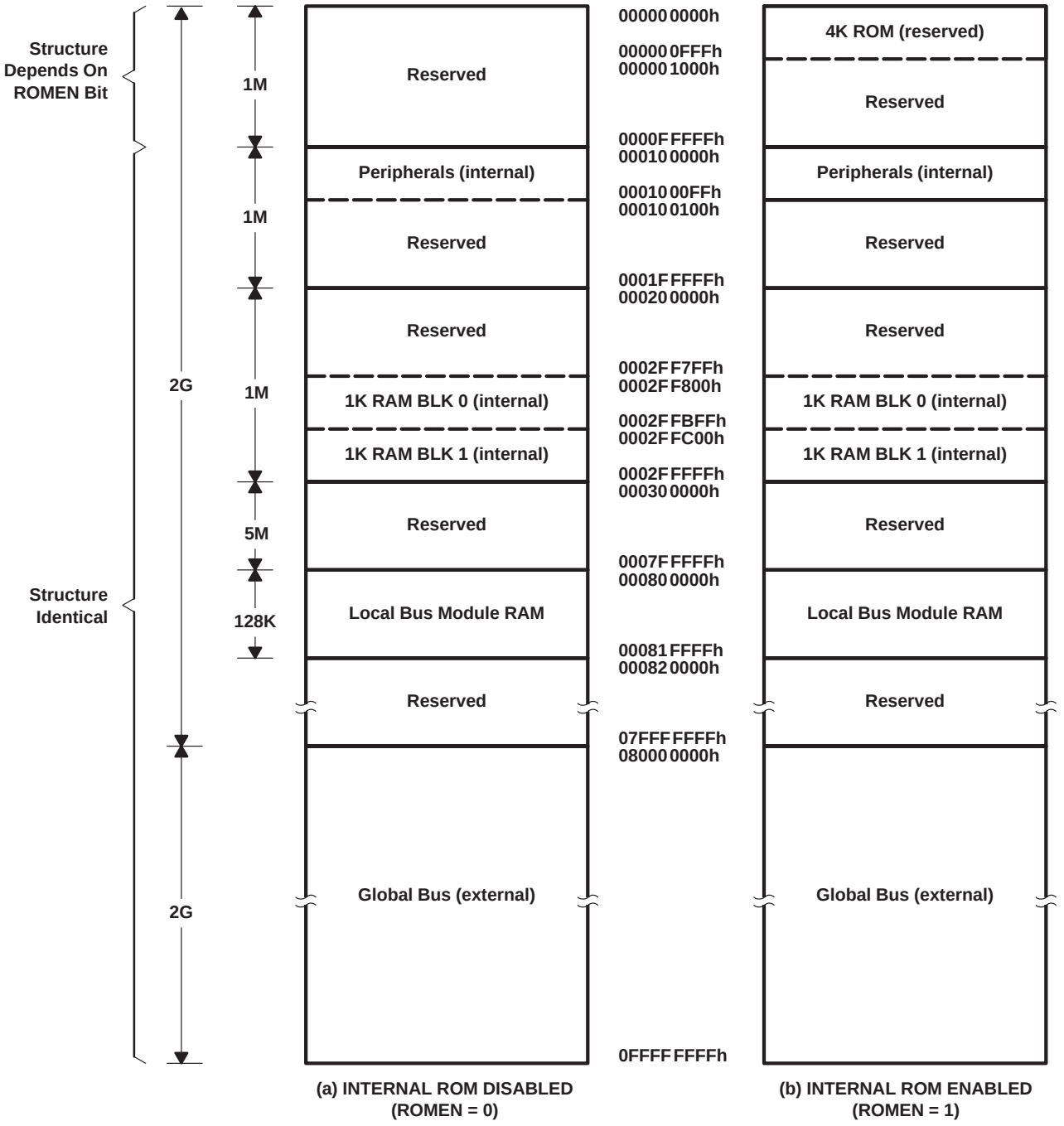


Figure 1. Memory Map for the ’C40 Within the Multichip Module

reference documentation and data sheet scope

The SMJ320MCM41D is qualified to MIL-PRF-38535. Electrical continuity of the module is ensured through use of IEEE-1149.1-compatible boundary-scan testing and functional checkout of local SRAM space.

KGD refers to Texas Instruments (TI™) known-good-die strategy. TI KGDs are fully tested over the military temperature range per MIL-PRF-38535 QML. Electrical testing ensures compliance of the ’C40 KGD components to the SMJ320C40 data sheet (literature number SGUS017) over the operating temperature range. The SMJ320MCM41D module timings are virtually unchanged from the SMJ320C40 data sheet timings. A SMJ320C40 data sheet is provided for customer reference only and does not imply MCM compliance to published timings.

For a complete description of the ’C40 operation and application information, refer to the *TMS320C4x User’s Guide* (literature number SPRU063).

capacitance

Capacitance of a single ’C40 die is specified by design to be 15 pF maximum for both inputs and outputs. Module networks add up to 25 pF. Simulation of die or substrate capacitance is performed after any design change. Power measurements taken for the ’C40 die are made with an additional 80-pF load capacitance. Refer to the SMJ320C40 data sheet (literature number SGUS017) for the test load circuit.

operational timings and module testing

TI processing ensures that operation is verified to the published data sheet specifications on the ’C40 in die form. All voltage, timing, speed, and temperature specifications are met before any die is placed into a multichip module. For this reason, it is unnecessary to verify all ’C40 voltage and timing parameters at the module level.

Characterization of the ’MCM41D substrate shows that the module performs as an equivalent system of discretely packaged ’C40 devices. This performance is ensured through a full-frequency functional checkout of the module that verifies selected worst-case timings. An additional propagation delay is introduced by the substrate. This value is assured by design to be less than 1 ns, but it is not tested. Refer to the SMJ320C40 data sheet (literature number SGUS017) for a complete listing of timing diagrams and limits.

module test capability (future compatibility)

The ’C40 supports the IEEE-1149.1 testability standard, and all test-access port (TAP) pins are brought out to the module footprint. This configuration allows users to test the module using third-party JTAG testability tools or other boundary-scan control software. Proper software configuration allows users to debug or launch code on the module via the ’C40 emulator and XDS™ pod. Both of these tools are used as a part of outgoing module testing.

The ’MCM41 supports third-party JTAG diagnostic families of products for verification and debug of boundary-scan circuits, boards, and systems. For further information on JTAG testability tools, please contact your local TI sales representative or authorized TI distributor.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . – 0.3 V to 7 V
Voltage range on any pin . . . . . – 0.3 V to 7 V
Output voltage range, V_O . . . . . – 0.3 V to 7 V
Operating free-air temperature range, T_A: L version (commercial) . . . . . 0°C to 70°C
M version (military) . . . . . –55°C to125°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_{IH}	High-level input voltage	CLKIN	2.6	V_{CC} + 0.3	V
		$\overline{\text{CSTRBx}}$, $\overline{\text{CRDYx}}$, $\overline{\text{CREQx}}$, $\overline{\text{CACKx}}$	2.2	V_{CC} + 0.3	
		All others inputs	2	V_{CC} + 0.3	
V_{IL}	Low-level input voltage		– 0.3	0.8	V
I_{OH}	High-level output current			– 300	µA
I_{OL}	Low-level output current			2	mA
T_A	Operating free-air temperature	L Version (Commercial)	0	70	°C
		M Version (Military)	– 55	125	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

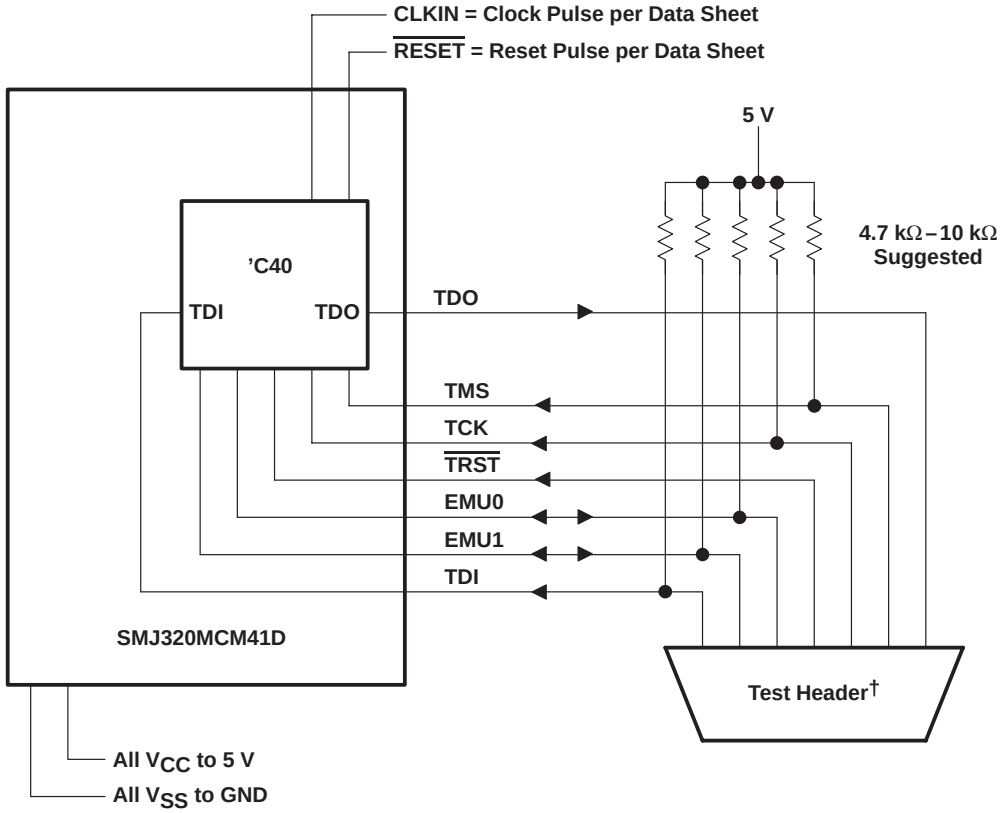
PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = MAX	2.4	3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = MAX		0.3	0.6	V
I_{CC}	Supply current	V_{CC} = MAX		0.4	0.6	A
I_Z	Three-state current	$V_I = V_{SS}$ to V_{CC}	– 20		20	µA
I_I	Input current	$V_I = V_{SS}$ to V_{CC}	– 10		10	µA
I_{IP}	Input current, internal pullup (see Note 2)	$V_I = V_{SS}$ to V_{CC}	– 400		30	µA
I_{IC}	Input current, CLKIN	$V_I = V_{SS}$ to V_{CC}	– 50		50	µA
I_{IPD}	Input current, internal pulldowns, $\overline{\text{TRST}}$	$V_I = V_{SS}$ to V_{CC}	– 20		400	µA

‡ For conditions shown as MIN / MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pins with internal pullup devices: TDI, TCK, TMS

module test circuit

Figure 2 illustrates the basic circuits for the ’MCM41D. Refer to the *TMS320C4x User’s Guide* (literature number SPRU063) for more detailed information.



† The test header normally consists of the XDS510™ for the ’C40 emulation or ASSET hardware for interconnect testing.

Figure 2. Sample Test Circuit

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XDS510 is a trademark of Texas Instruments Incorporated.

thermal analysis

Thermal conduction of components in the SMJ320MCM41D is dependent on the thermal resistance of the material under each die as well as the die area thermally connected to the heat-dissipating medium. Since these properties vary with layout and die size, ’C40 and SRAM components should be considered separately. The following table lists primary parameters required for thermal analysis of the module. The junction temperature, T_J, is not to be exceeded for the ’C40 or the SRAM die.

primary parameters required for thermal analysis of the SMJ320MCM41D module

PARAMETER		ALTERNATE SYMBOL	MIN	TYP	MAX	UNIT
T_J	Junction temperature under operating condition	T_J			150	°C
P_{MCM}	Single MCM power dissipation	P_{MCM}		2.0	5.2	W
Z_{0JC}	Thermal impedance (junction-to-case) of package	T_{jc}		1.3		°C/W
Z_{0JA}	Thermal impedance (junction-to-ambient air, 0 cfm) of package	T_{ja}		28.0		°C/W
T_{SOL}	Maximum solder temperature (10 s duration)	T_{SOL}			260	°C

power estimation

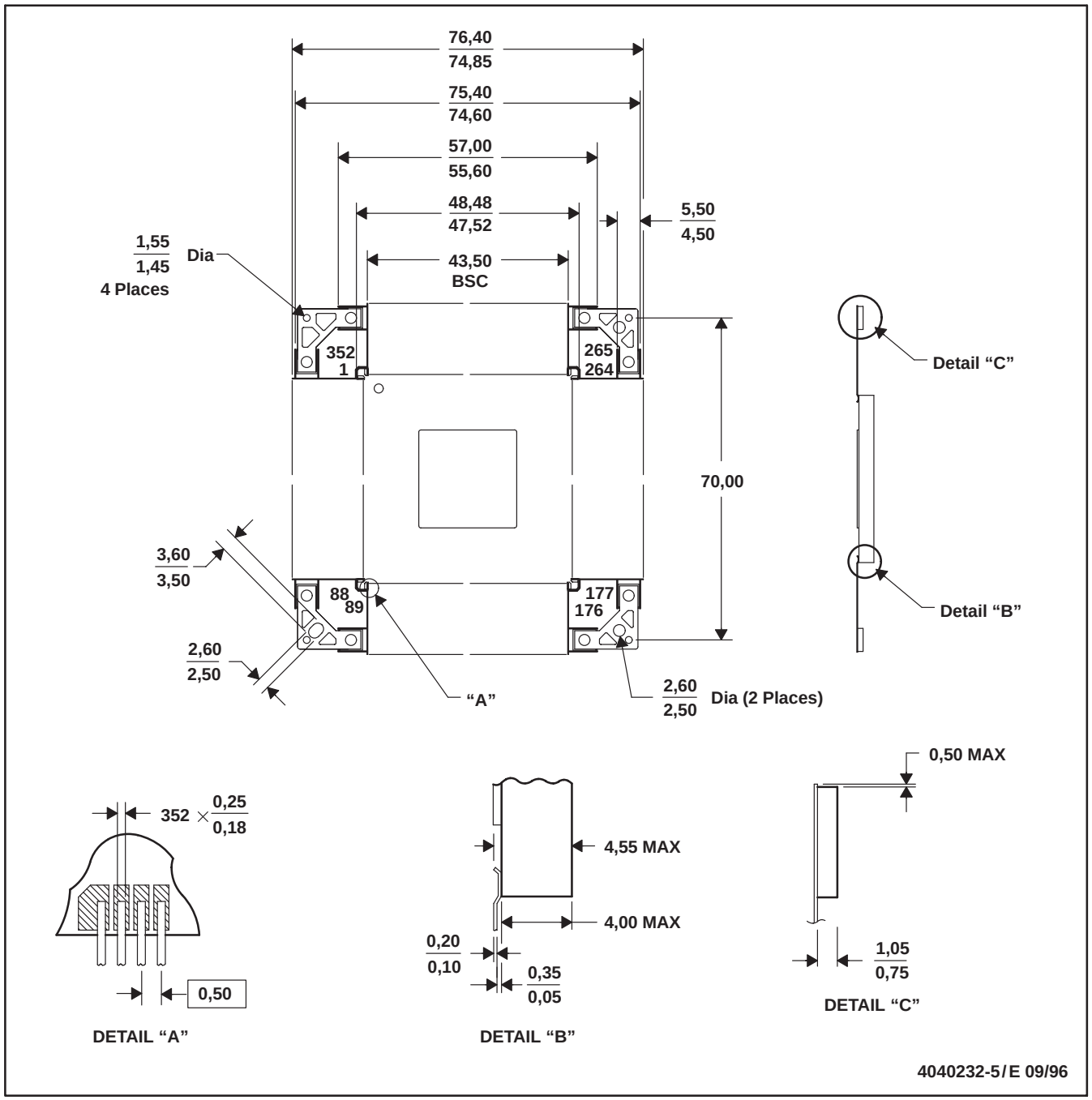
The power requirements of the ’320MCM41 have been characterized over the operating temperature range. See the application report *Calculation of TMS320C40 Power Dissipation* (literature number SPRA032) as reference for power estimation of the ’C40 components.

Typical power dissipation has been measured with the ’C40s executing a 64-point Fast Fourier Transform (FFT) algorithm. Input and output data arrays resided in module SRAM, and output data was written out to the global-address space. The global databus was loaded with 80-pF test loads, and both local and global writes were configured for zero-wait-state memory. Under typical conditions of 25°C, 5-V V_{CC}, and 40-MHz CLKIN frequency, the power dissipation was measured to be 1.75 W.

Maximum power dissipation has been measured under worst-case conditions. The global databus was loaded with 80-pF test loads, and simultaneous zero-wait-state writes have been performed to both local and global buses. Under worst-case conditions of – 55°C, 5.25-V V_{CC}, and 40-MHz CLKIN frequency, the power dissipation was determined to be 3 W. The algorithm executed during these tests consists of parallel writes of alternating 0xAAs and 0x55s to both local SRAM and global-address spaces. This algorithm is not considered to be a practical use of the ’C40’s resources; therefore, the associated power measurement should be considered absolute maximum only.

MECHANICAL DATA

HFH (S-CQFP-F352) **CERAMIC QUAD FLATPACK WITH NCTB**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MO-134 AE

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