

1.5SMC6.8AT3 Series, SZ1.5SMC6.8AT3 Series

1500 Watt Peak Power Zener Overvoltage Suppressors

Unidirectional*

The SMC series is designed to protect voltage sensitive components from high voltage, high energy transients. They have excellent clamping capability, high surge capability, low zener impedance and fast response time. The SMC series is supplied in ON Semiconductor's exclusive, cost-effective, highly reliable SURMETIC® package and is ideally suited for use in communication systems, automotive, numerical controls, process controls, medical equipment, business machines, power supplies and many other industrial/consumer applications.

Specification Features

- Working Peak Reverse Voltage Range – 5.8 to 77.8 V
- Standard Zener Breakdown Voltage Range – 6.8 to 91 V
- Peak Power – 1500 W @ 1.0 ms
- ESD Rating of Class 3 (>16 kV) per Human Body Model
- Maximum Clamp Voltage @ Peak Pulse Current
- Low Leakage < 5.0 μ A Above 10 V
- UL 497B for Isolated Loop Circuit Protection
- Maximum Temperature Coefficient Specified
- Response Time is Typically < 1.0 ns
- AEC-Q101 Qualified and PPAP Capable
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- Pb-Free Packages are Available**

Mechanical Characteristics

CASE: Void-free, transfer-molded, thermosetting plastic

FINISH: All external surfaces are corrosion resistant and leads are readily solderable

MAXIMUM CASE TEMPERATURE FOR SOLDERING PURPOSES:
260°C for 10 Seconds

LEADS: Modified L-Bend providing more contact area to bond pads

POLARITY: Cathode indicated by molded polarity notch

MOUNTING POSITION: Any

* Bidirectional devices will not be available in this series.

**For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



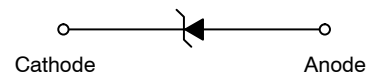
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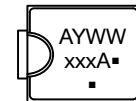
**PLASTIC SURFACE MOUNT
ZENER OVERVOLTAGE
TRANSIENT SUPPRESSORS
5.8 – 78 VOLTS
1500 WATT PEAK POWER**



SMC
CASE 403
PLASTIC



MARKING DIAGRAM



- xxxA = Specific Device Code
(See Table on Page 3)
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device***	Package	Shipping†
1.5SMCxxxAT3	SMC	2,500 / Tape & Reel
1.5SMCxxxAT3G	SMC (Pb-Free)	2,500 / Tape & Reel
SZ1.5SMCxxxAT3G	SMC (Pb-Free)	2,500 / Tape & Reel

***The "T3" suffix refers to a 13 inch reel.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Individual devices are listed on page 3 of this data sheet.

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation (Note 1) @ $T_L = 25^\circ\text{C}$, Pulse Width = 1 ms	P_{PK}	1500	W
DC Power Dissipation @ $T_L = 75^\circ\text{C}$ Measured Zero Lead Length (Note 2) Derate Above 75°C	P_D	4.0	W
Thermal Resistance, Junction-to-Lead	$R_{\theta JL}$	54.6 18.3	mW/ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$
DC Power Dissipation (Note 3) @ $T_A = 25^\circ\text{C}$ Derate Above 25°C	P_D	0.75	W
Thermal Resistance from Junction-to-Ambient	$R_{\theta JA}$	6.1 165	mW/ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$
Forward Surge Current (Note 4) @ $T_A = 25^\circ\text{C}$	I_{FSM}	200	A
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

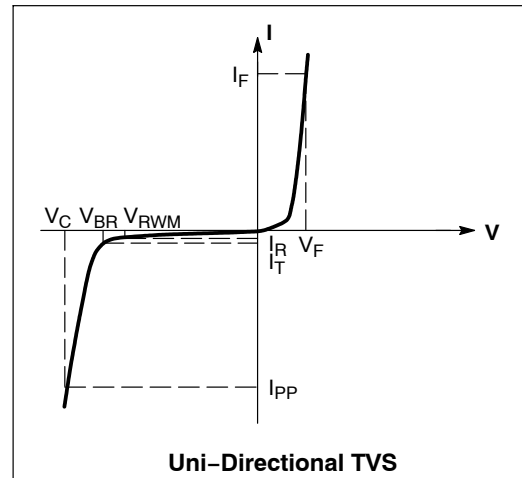
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 10 X 1000 μs , non-repetitive
- 1 in. square copper pad, FR-4 board
- FR-4 board, using ON Semiconductor minimum recommended footprint, as shown in 403 case outline dimensions spec.
- 1/2 sine wave (or equivalent square wave), PW = 8.3 ms, duty cycle = 4 pulses per minute maximum.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, $V_F = 3.5\text{ V Max.}$ @ I_F (Note 5) = 100 A)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
ΘV_{BR}	Maximum Temperature Coefficient of V_{BR}
I_F	Forward Current
V_F	Forward Voltage @ I_F

- 1/2 sine wave or equivalent, PW = 8.3 ms non-repetitive duty cycle



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ELECTRICAL CHARACTERISTICS (Devices listed in *bold, italic* are ON Semiconductor Preferred devices.)

Device*	Device Marking	V _{RWM} (Note 6) V	I _R @ V _{RWM} μA	Breakdown Voltage				V _C @ I _{PP} (Note 8)		θV _{BR} %/°C
				V _{BR} V (Note 7)			@ I _T	V _C	I _{PP}	
				Min	Nom	Max	mA	V	A	
1.5SMC6.8AT3, G	6V8A	5.8	1000	6.45	6.8	7.14	10	10.5	143	0.057
1.5SMC7.5AT3, G	7V5A	6.4	500	7.13	7.5	7.88	10	11.3	132	0.061
1.5SMC8.2AT3, G	8V2A	7.02	200	7.79	8.2	8.61	10	12.1	124	0.065
1.5SMC9.1AT3	9V1A	7.78	50	8.65	9.1	9.55	1	13.4	112	0.068
1.5SMC10AT3	10A	8.55	10	9.5	10	10.5	1	14.5	103	0.073
1.5SMC11AT3	11A	9.4	5	10.5	11	11.6	1	15.6	96	0.075
1.5SMC12AT3, G	12A	10.2	5	11.4	12	12.6	1	16.7	90	0.078
1.5SMC13AT3, G	13A	11.1	5	12.4	13	13.7	1	18.2	82	0.081
SZ/1.5SMC15AT3, G	15A	12.8	5	14.3	15	15.8	1	21.2	71	0.084
SZ/1.5SMC16AT3, G	16A	13.6	5	15.2	16	16.8	1	22.5	67	0.086
1.5SMC18AT3, G	18A	15.3	5	17.1	18	18.9	1	25.2	59.5	0.088
SZ/1.5SMC20AT3, G	20A	17.1	5	19	20	21	1	27.7	54	0.09
1.5SMC22AT3, G	22A	18.8	5	20.9	22	23.1	1	30.6	49	0.092
1.5SMC24AT3, G	24A	20.5	5	22.8	24	25.2	1	33.2	45	0.094
SZ/1.5SMC27AT3, G	27A	23.1	5	25.7	27	28.4	1	37.5	40	0.096
SZ/1.5SMC30AT3, G	30A	25.6	5	28.5	30	31.5	1	41.4	36	0.097
SZ/1.5SMC33AT3, G	33A	28.2	5	31.4	33	34.7	1	45.7	33	0.098
SZ/1.5SMC36AT3, G	36A	30.8	5	34.2	36	37.8	1	49.9	30	0.099
SZ/1.5SMC39AT3, G	39A	33.3	5	37.1	39	41	1	53.9	28	0.1
SZ/1.5SMC43AT3, G	43A	36.8	5	40.9	43	45.2	1	59.3	25.3	0.101
SZ/1.5SMC47AT3, G	47A	40.2	5	44.7	47	49.4	1	64.8	23.2	0.101
SZ/1.5SMC51AT3, G	51A	43.6	5	48.5	51	53.6	1	70.1	21.4	0.102
1.5SMC56AT3, G	56A	47.8	5	53.2	56	58.8	1	77	19.5	0.103
SZ/1.5SMC62AT3, G	62A	53	5	58.9	62	65.1	1	85	17.7	0.104
1.5SMC68AT3, G	68A	58.1	5	64.6	68	71.4	1	92	16.3	0.104
1.5SMC75AT3, G	75A	64.1	5	71.3	75	78.8	1	103	14.6	0.105
1.5SMC82AT3, G	82A	70.1	5	77.9	82	86.1	1	113	13.3	0.105
1.5SMC91AT3, G	91A	77.8	5	86.5	91	95.5	1	125	12	0.106

Devices listed in *bold, italic* are ON Semiconductor Preferred devices. Preferred devices are recommended choices for future use and best overall value.

6. A transient suppressor is normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal to or greater than the DC or continuous peak operating voltage level.

7. V_{BR} measured at pulse test current I_T at an ambient temperature of 25°C.

8. Surge current waveform per Figure 2 and derate per Figure 3 of the General Data – 1500 Watt at the beginning of this group.

*The "G" suffix indicates Pb-Free package available.

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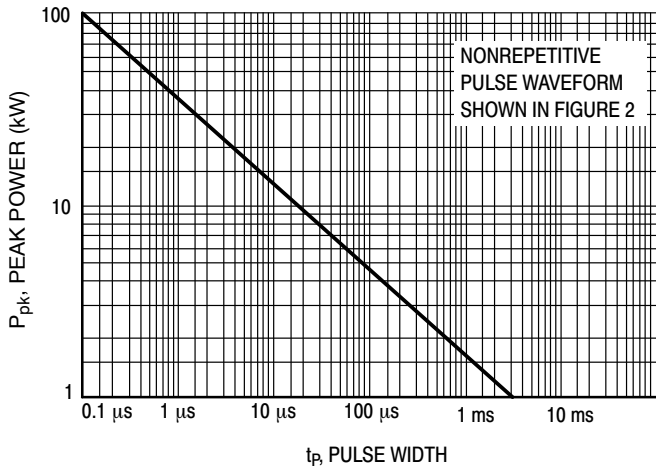


Figure 1. Pulse Rating Curve

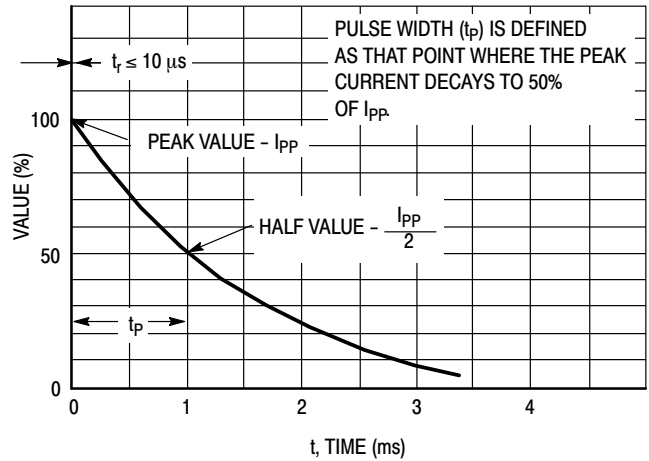


Figure 2. Pulse Waveform

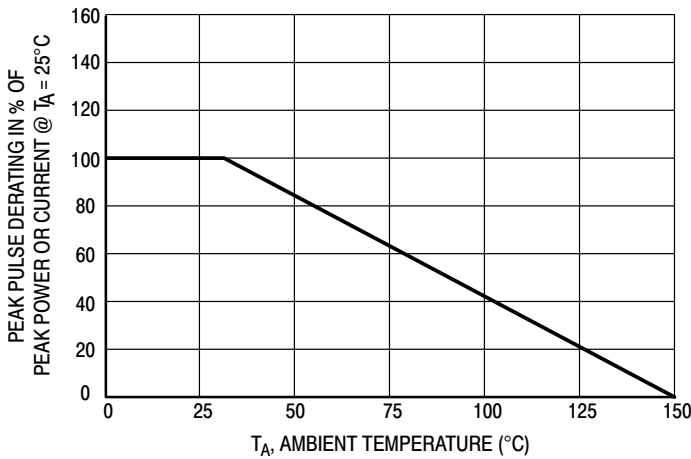


Figure 3. Pulse Derating Curve

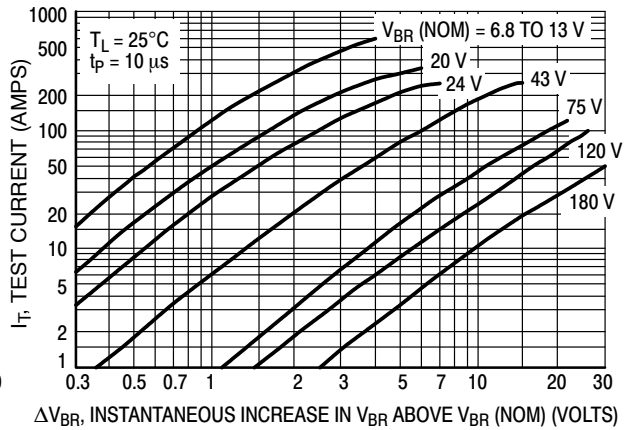


Figure 4. Dynamic Impedance

UL RECOGNITION

The entire series has *Underwriters Laboratory Recognition* for the classification of protectors (QVGQ2) under the UL standard for safety 497B and File #E210057. Many competitors only have one or two devices recognized or have recognition in a non-protective category. Some competitors have no recognition at all. With the UL497B recognition, our parts successfully passed several tests

including Strike Voltage Breakdown test, Endurance Conditioning, Temperature test, Dielectric Voltage-Withstand test, Discharge test and several more.

Whereas, some competitors have only passed a flammability test for the package material, we have been recognized for much more to be included in their Protector category.

APPLICATION NOTES

RESPONSE TIME

In most applications, the transient suppressor device is placed in parallel with the equipment or component to be protected. In this situation, there is a time delay associated with the capacitance of the device and an overshoot condition associated with the inductance of the device and the inductance of the connection method. The capacitive effect is of minor importance in the parallel protection scheme because it only produces a time delay in the transition from the operating voltage to the clamp voltage as shown in Figure 5.

The inductive effects in the device are due to actual turn-on time (time required for the device to go from zero current to full current) and lead inductance. This inductive effect produces an overshoot in the voltage across the equipment or component being protected as shown in Figure 6. Minimizing this overshoot is very important in the application, since the main purpose for adding a transient suppressor is to clamp voltage spikes. The SMC series have a very good response time, typically < 1.0 ns and negligible inductance. However, external inductive effects could produce unacceptable overshoot. Proper circuit layout,

minimum lead lengths and placing the suppressor device as close as possible to the equipment or components to be protected will minimize this overshoot.

Some input impedance represented by Z_{in} is essential to prevent overstress of the protection device. This impedance should be as high as possible, without restricting the circuit operation.

DUTY CYCLE DERATING

The data of Figure 1 applies for non-repetitive conditions and at a lead temperature of 25°C. If the duty cycle increases, the peak power must be reduced as indicated by the curves of Figure 7. Average power must be derated as the lead or ambient temperature rises above 25°C. The average power derating curve normally given on data sheets may be normalized and used for this purpose.

At first glance the derating curves of Figure 7 appear to be in error as the 10 ms pulse has a higher derating factor than the 10 μ s pulse. However, when the derating factor for a given pulse of Figure 7 is multiplied by the peak power value of Figure 1 for the same pulse, the results follow the expected trend.

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TYPICAL PROTECTION CIRCUIT

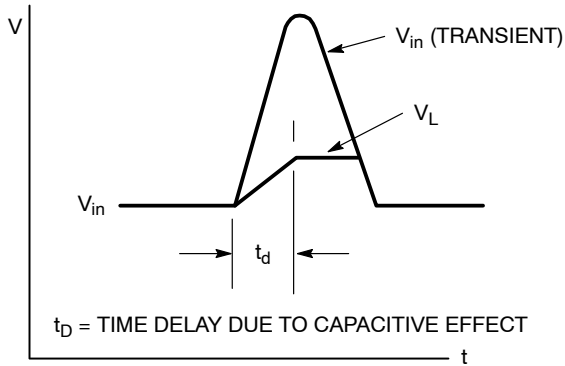
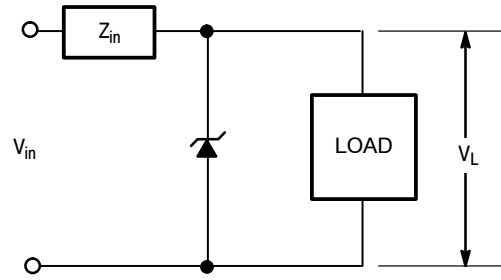


Figure 5.

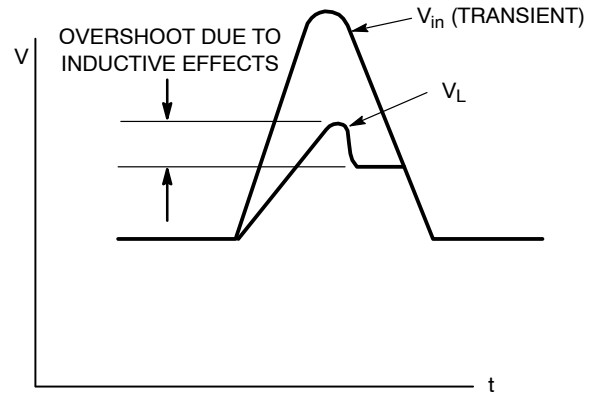


Figure 6.

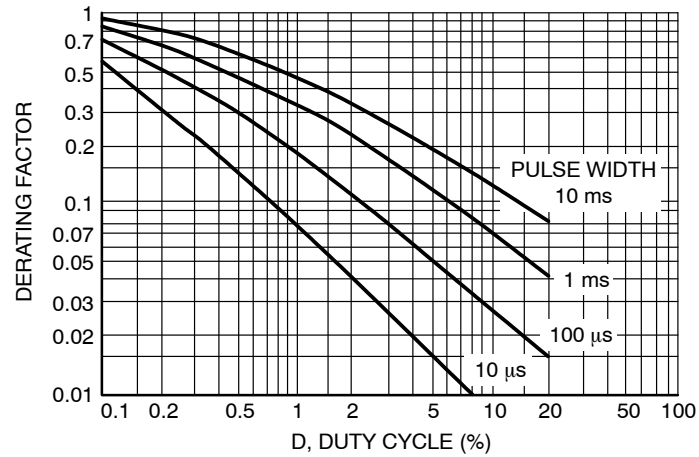
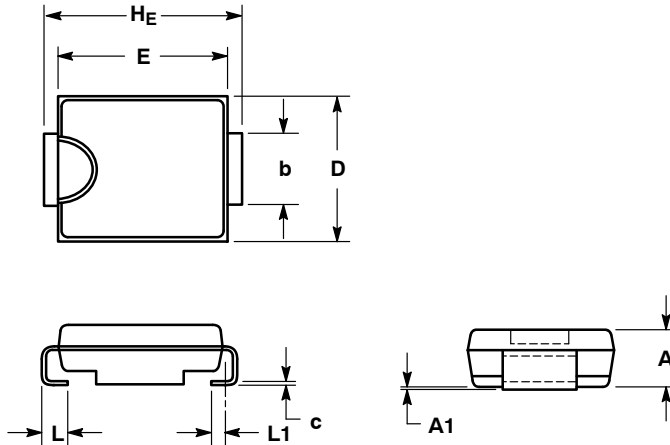


Figure 7. Typical Derating Factor for Duty Cycle

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PACKAGE DIMENSIONS

SMC
CASE 403-03
ISSUE E

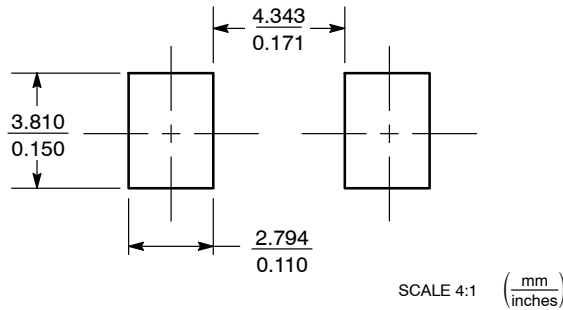


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.
4. 403-01 THRU -02 OBSOLETE, NEW STANDARD 403-03.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.90	2.13	2.41	0.075	0.084	0.095
A1	0.05	0.10	0.15	0.002	0.004	0.006
b	2.92	3.00	3.07	0.115	0.118	0.121
c	0.15	0.23	0.30	0.006	0.009	0.012
D	5.59	5.84	6.10	0.220	0.230	0.240
E	6.60	6.86	7.11	0.260	0.270	0.280
HE	7.75	7.94	8.13	0.305	0.313	0.320
L	0.76	1.02	1.27	0.030	0.040	0.050
L1	0.51 REF			0.020 REF		

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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